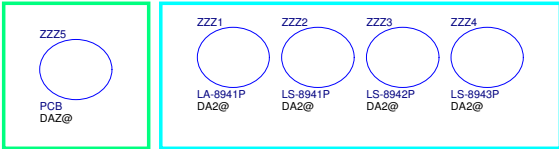


Compal Confidential
Model Name : Q1VZC
File Name :LA-8941P
BOM P/N:43



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Q1VZC M/B Schematics Document

Intel Sandy Bridge ULV Processor + Panther Point PCH

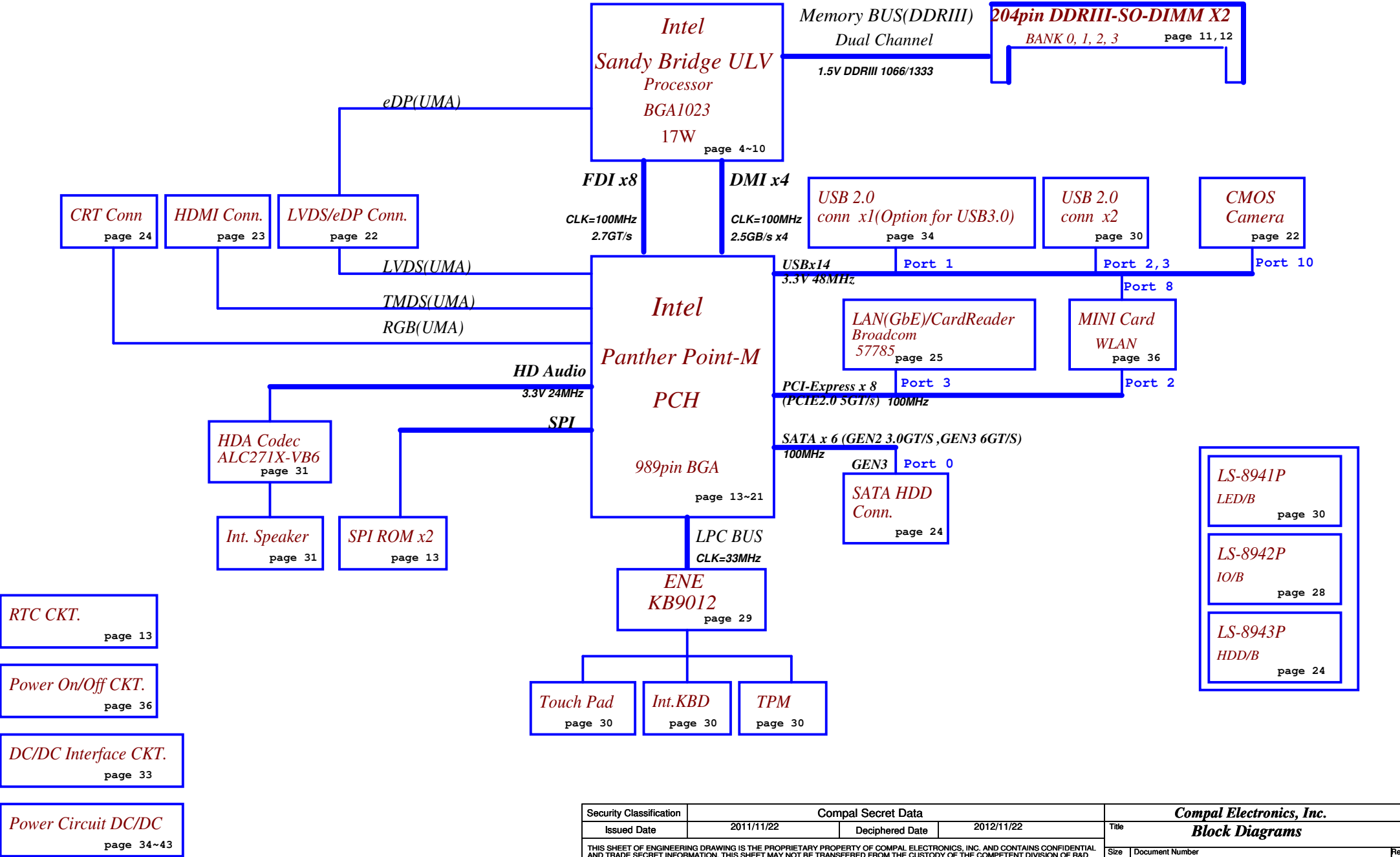
2012-04-19

REV:1.0

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			Document Number	Rev
			Q1VZC M/B LA-8941P Schematic	1.0
			Date: Friday, April 20, 2012	Sheet 1 of 45

Compal Confidential

Model Name : Q1VZC
File Name :LA-8941P



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH (Short Jump)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VREF_SUS	+5VALW to +5VREF_SUS power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

PCH SM Bus address

Device	Address
ChannelA	DIMM0 A0 1010 000X JDIMM1(STD)
ChannelB	DIMM0 B0 1010 010X JDIMM2(REV)

schematic-laptop.blogspot.com

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

USB Port Table

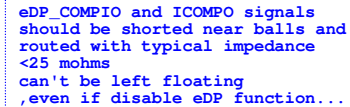
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	
		1	USB 2.0(Options for USB3.0)
	UHCI1	2	USB port(Left 2.0)
		3	USB Port(Left 2.0)
	UHCI2	4	
		5	
EHCI2	UHCI3	6	
		7	
	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	Camera
		11	
	UHCI6	12	
		13	













BTO Option Table

BTO Item	BOM Structure
Celeron 867	C867@
Pentium 977	P977@
Unpop	@
eDP Panel	EDP@
LVDS Panel	LVDS@
Connector	CONN@
USB3 Only	USB3@
Deep S3	DS3@
Normal S3	S3@
Intel i5/i7 CPU only	I57@
Celeron/Pentium/i3 CPU only	CP3@

USB 3.0	Port	
XHCI	1	
	2	USB Port(Right 3.0)
	3	
	4	

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Date: Friday, April 20, 2012				Sheet 3 of 45	

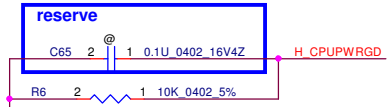


<p>UCPU1</p>  <p>AV8062701147701 P977@</p> <p>SA00005BJ50</p>	<p>UCPU1</p>  <p>AV8062701047504 I2467@</p> <p>SA00004X010</p>	<p>UCPU1</p>  <p>AV8062701047904 I2367@</p> <p>SA000051H60</p>	<p>UCPU1</p>  <p>AV8062701148001 C877@</p> <p>SA00005QI40</p>	<p>HR(Sandy Bridge)</p>
<p>UCPU1</p>  <p>AV8062701147601 P987@</p> <p>SA00005QH50</p>	<p>UCPU1</p>  <p>AV8062701147801 P967@</p> <p>SA000051J40</p>	<p>UCPU1</p>  <p>AV8062701048004 I2377@</p> <p>SA00005MX60</p>		
<p>UCPU1</p>  <p>AV8063801058002 I3317@</p> <p>SA00005K6B0</p>	<p>UCPU1</p>  <p>AV8063801057405 I3667@</p> <p>SA00005LAA0</p>	<p>UCPU1</p>  <p>AV8063801058401 I3217@</p> <p>SA00005L5C0</p>		<p>CR(Ivy Bridge)</p>
<p>UCPU1</p>  <p>AV8063801057801 I3427@</p> <p>SA00005L9B0</p>	<p>UCPU1</p>  <p>AV8063801057605 I3517@</p> <p>SA00005K5B0</p>			

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				Custom	Q1VZC M/B LA-8941P Schematic	1.0
				Date:	Friday, April 20, 2012	Sheet 4 of 45

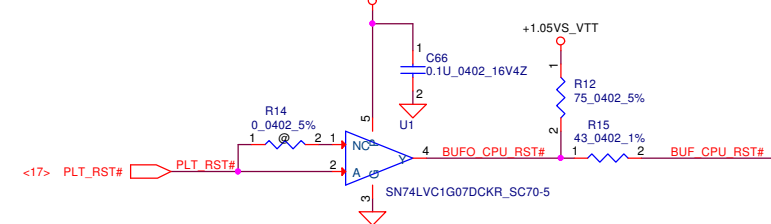
PCH->CPU
UNCOREPWROK:非CORE外的電OK
SM_DRAMPWROK:DRAM power ok
RESET#:都ok後請CPU做reset

Follow DG 1.5& Tacoma_Fall2 1.0



Follow DG 1.5 & Tacoma_Fall2 1.0
Buffered reset to CPU

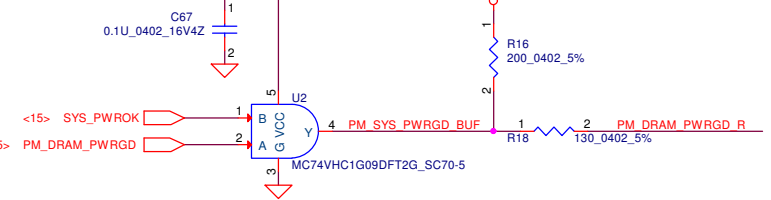
Use open drain logic gate:
+1.05VS_VTT PU pop 75ohm
series resistor pop 43ohm



RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma_Fall2 1.0

Use open drain logic gate:
+1.5V_CPU_VDDQ PU pop 200ohm
series resistor pop 130ohm



PROC_SELECT#
PH VCPLL and connect to PCH DF_TV5

偵測CPU有無安裝

XBOX 三缸功能

follow Checklist 1.5

<18,29> H_PECI

<18> H_THRMTRIP#

<15> H_PM_SYNC

<18> H_CPUPWRGD

<15> SYS_PWROK

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

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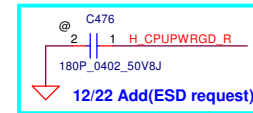
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<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD

<15> PM_DRAMPWRGD



12/22 Add(ESD request)

UCPU1B

PROC_SELECT#

PROC_DETECT#

CATERR#

PECI

PROCHOT#

THERMTRIP#

PM_SYNC

UNCOREPWROK

SM_DRAMPWROK

RESET#

IVY-BRIDGE_BGA1023

C867@

MISC

THERMAL

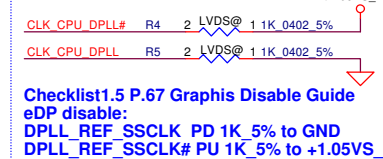
PWR MANAGEMENT

CLOCKS

DDR3

JTAG & BPM

0921 LVDS@->@



Checklist 1.5 P.67 Graphis Disable Guide

eDP disable:

DPLL_REF_SSCLK PD 1K 5% to GND

DPLL_REF_SSCLK# PU 1K 5% to +1.05VS_VTT

SM_RCOMP0,SM_RCOMP1

W=20mil L=500mil S=13mil

SM_RCOMP2

W=15mil L=500mil S=13mil

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

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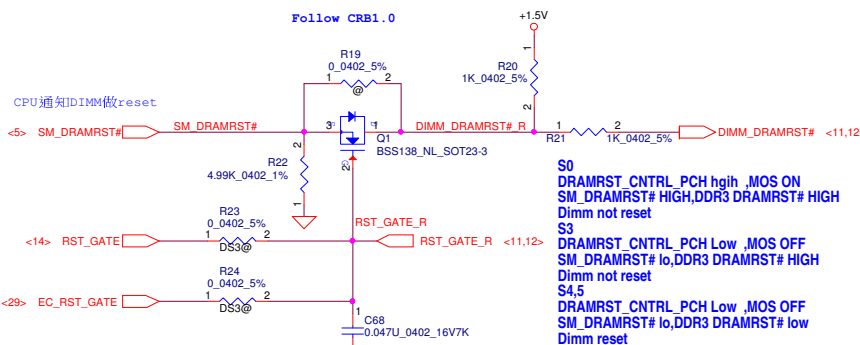
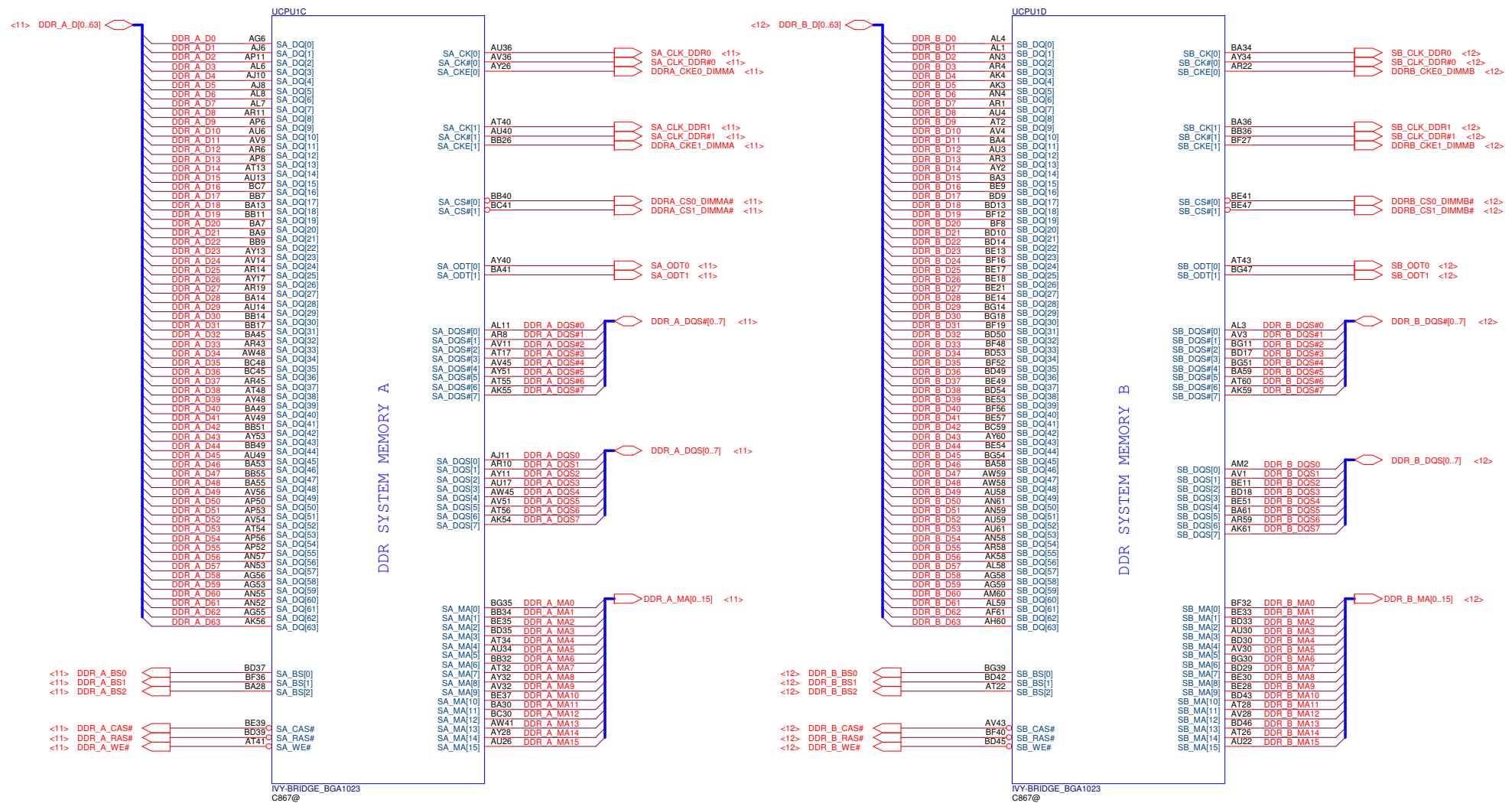
SM_DRAMRST#

SM_DRAMRST#

SM_DRAMRST#

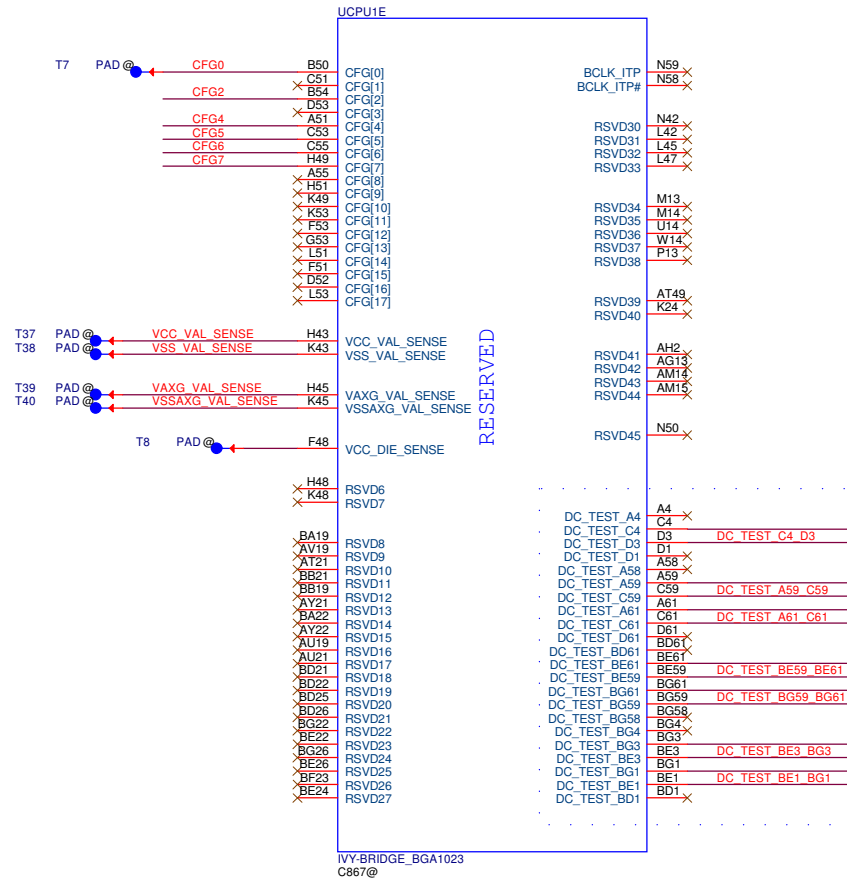
SM_DRAMRST#

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Size Custom	Document Number	Q1VZC M/B LA-8941P Schematic		Rev 1.0
Date:	Friday, April 20, 2012	Sheet	5 of 45	

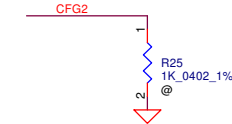


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Issued Date		Deciphered Date		PROCESSOR(3/7) DDRIII	
2011/11/22		2012/11/22		Title	
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		Q1VZC M/B LA-8941P Schematic		1.0	
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CFG Straps for Processor

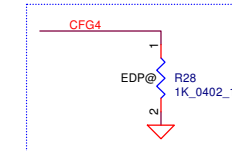


These pins are for solder joint reliability and non-critical to function. For BGA only.



PEG Static Lane Reversal - CFG2 is for the 16x

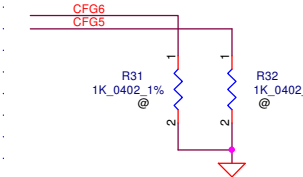
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed
------	--



UMA, Optimus eDP 啟動
DISO eDP 關閉

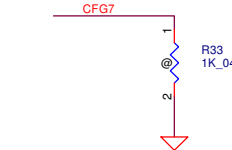
eDP enable

CFG4	★ 1: Disable 0: Enable
------	---------------------------



PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) 1x16 PCI Express ★ 10: 2x8 PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express
----------	---



PEG DEFER TRAINING

Tacoma_Fall2 1.0 P.12

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

INTEL Recommend VCC
4*470UF,12*22uF(0805) and 35*2.2uF(0402)
PD0.8
CAP at P.51

INTEL Recommend VCCIO
2*330UF,10*10uF(0603) and 26*1uF(0402)
PD0.8
CAP at P.51

ulv type
DC 33A

CORE SUPPLY

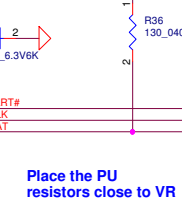
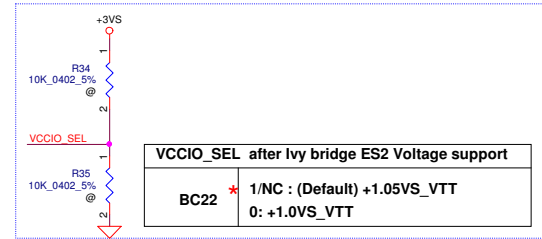
PEG IO AND DDR IO

QUIET
RAILS

SVID

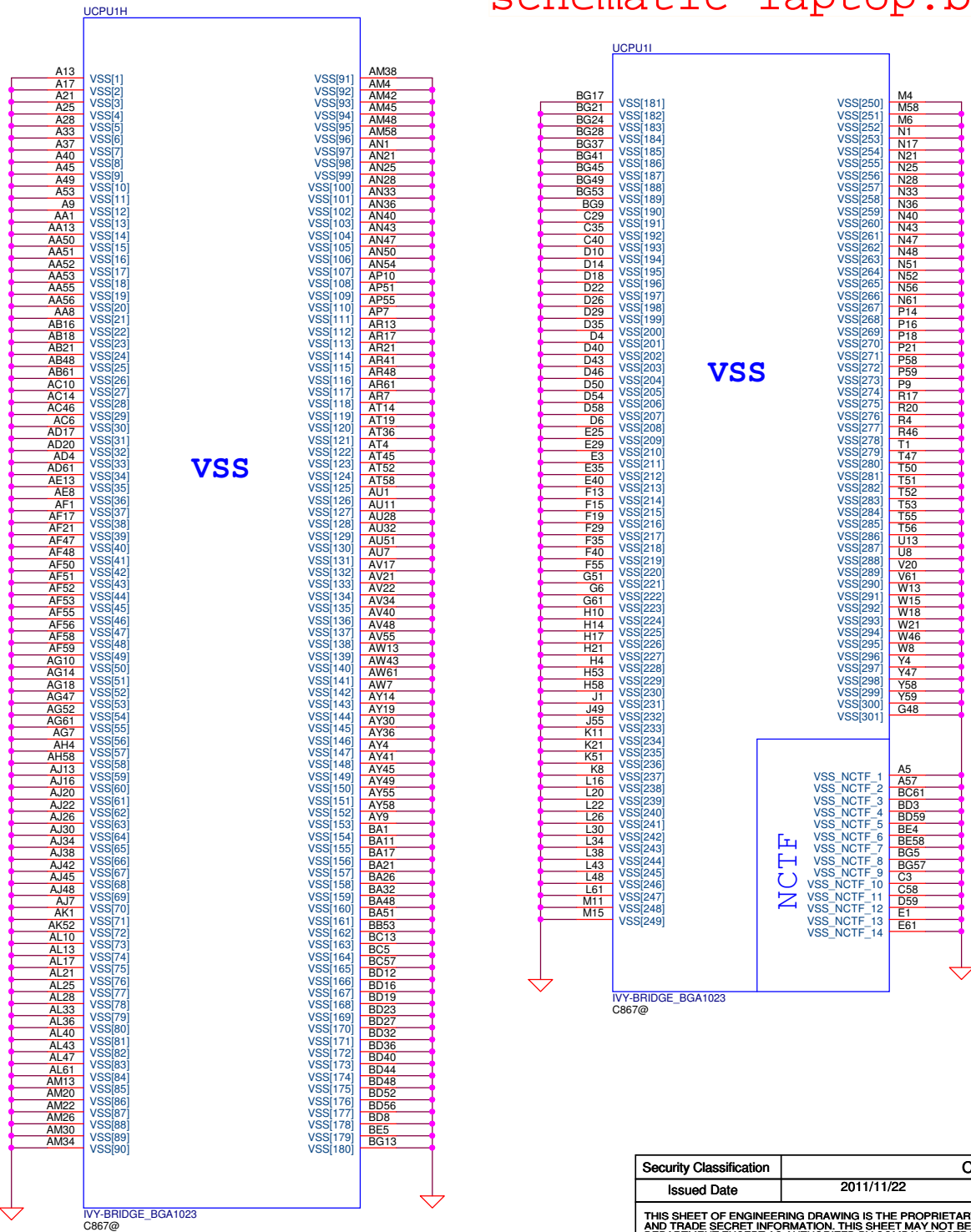
SENSE LINES

IVY-BRIDGE_BGA1023
C867@



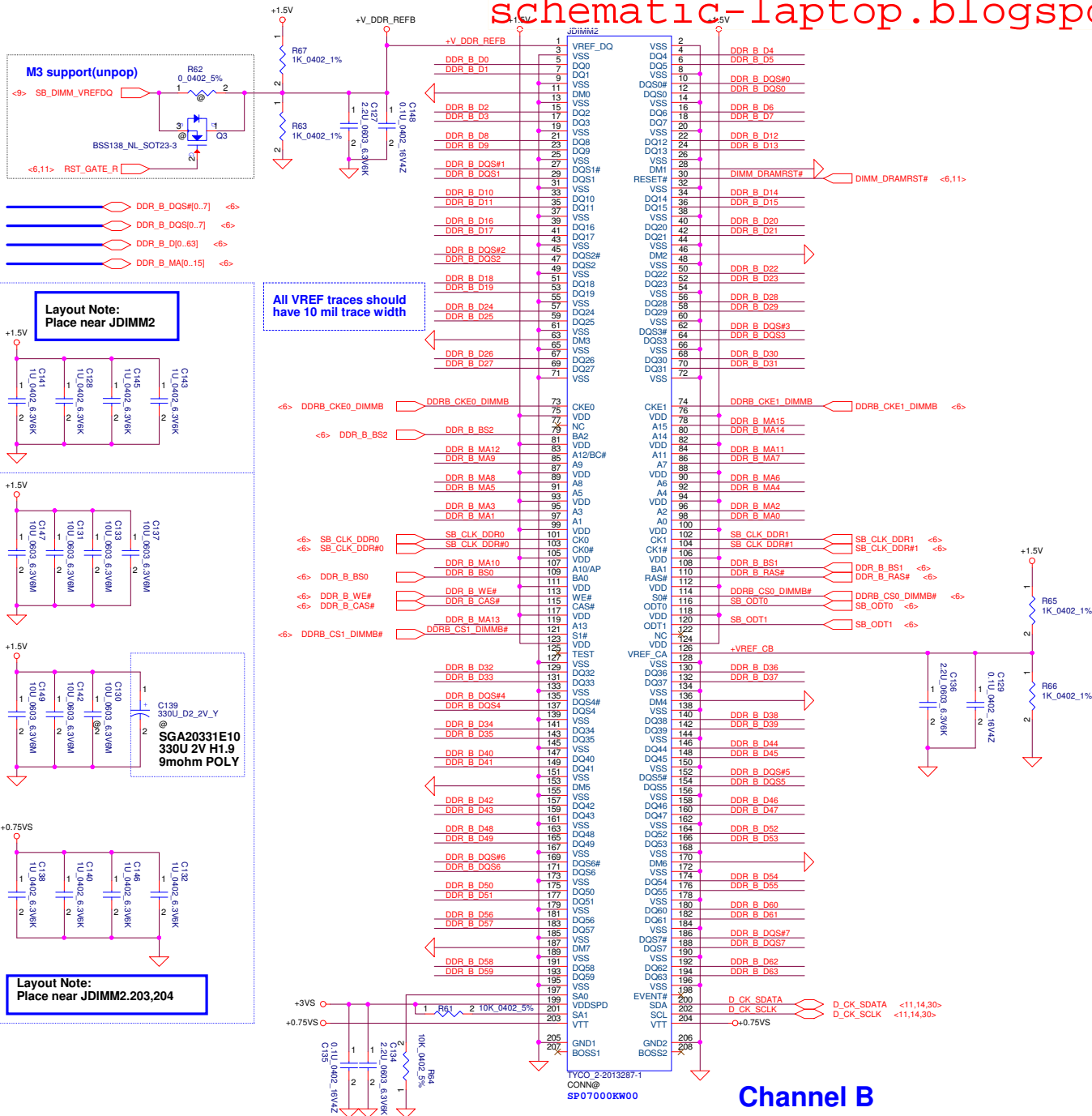
Should change to connect form power circuit & layout differential with VCCIO_SENSE.

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				Date	Q1V2C M/B LA-8941P Schematic	1.0
				Created	Friday, April 20, 2012	Sheet 11 of 45

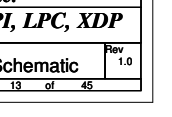
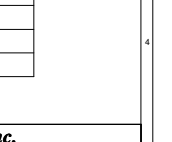
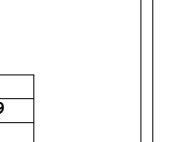
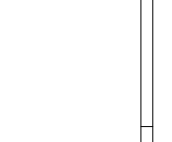
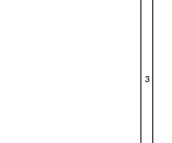
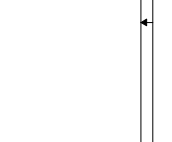
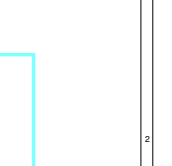
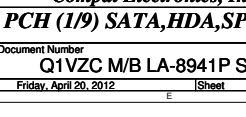
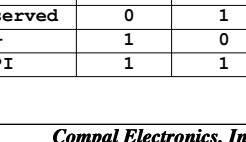
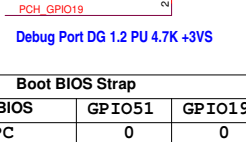
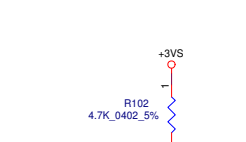
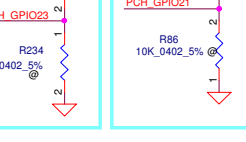
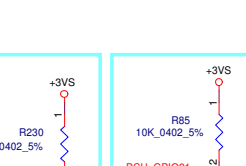
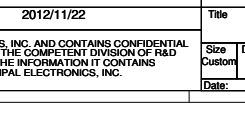
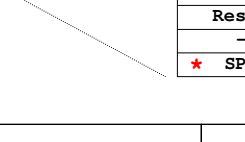
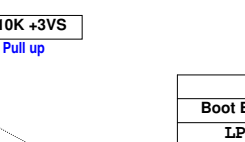
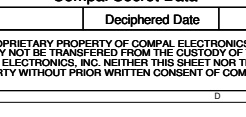
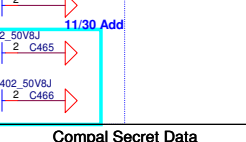
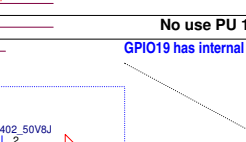
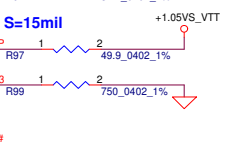
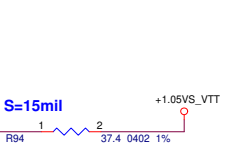
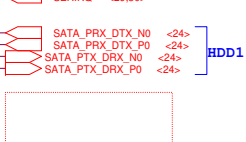
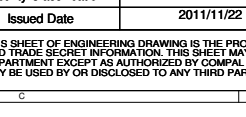
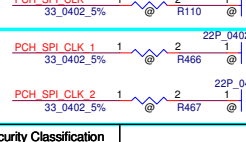
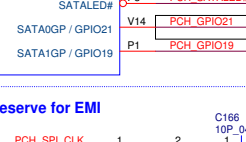
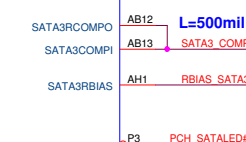
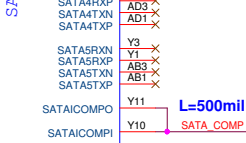
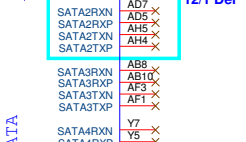
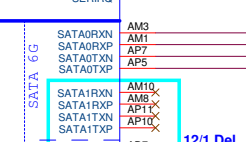
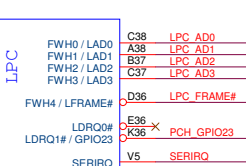
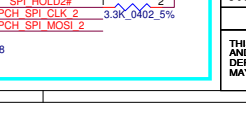
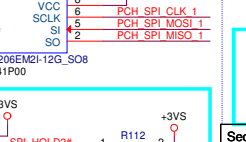
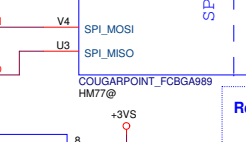
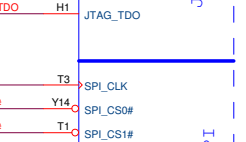
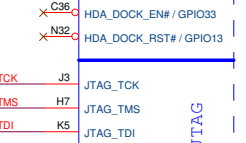
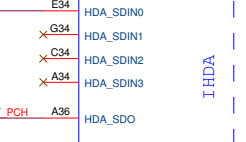
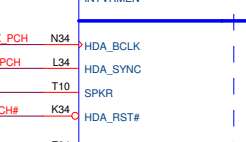
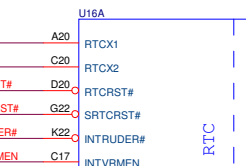
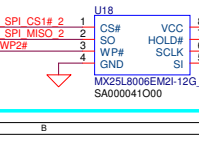
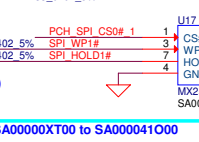
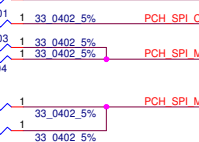
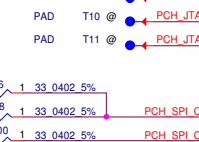
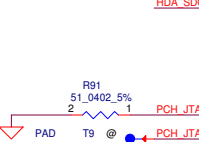
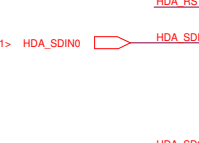
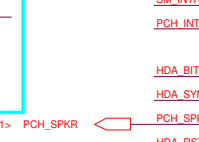
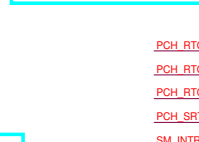
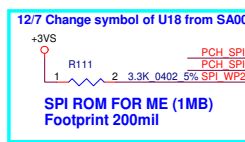
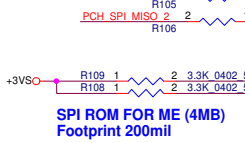
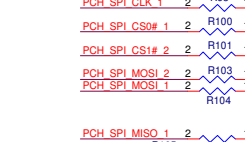
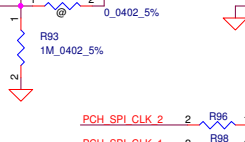
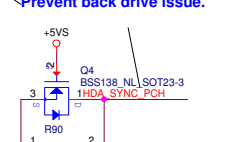
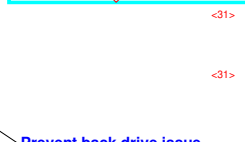
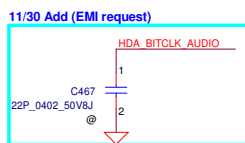
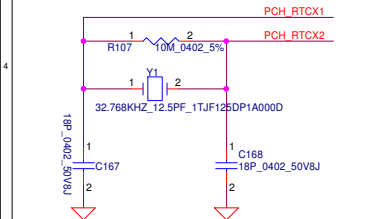
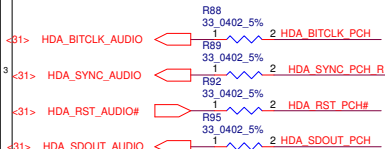
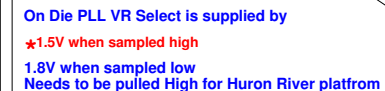
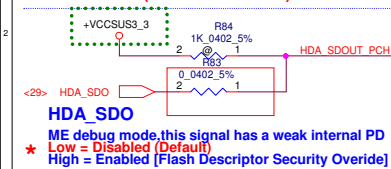
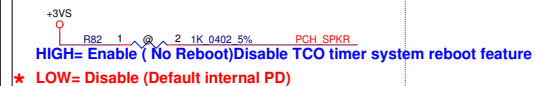
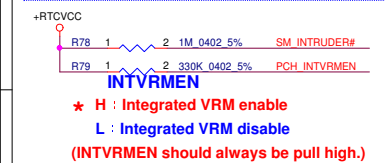
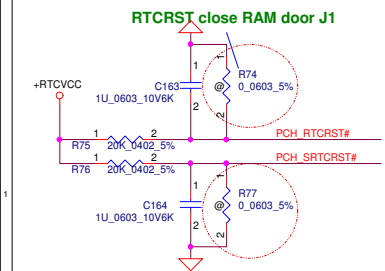


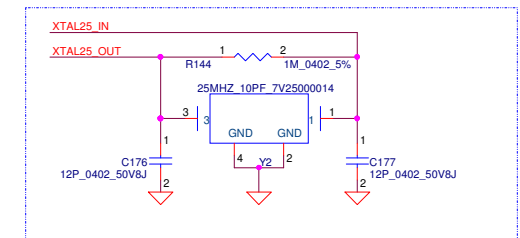
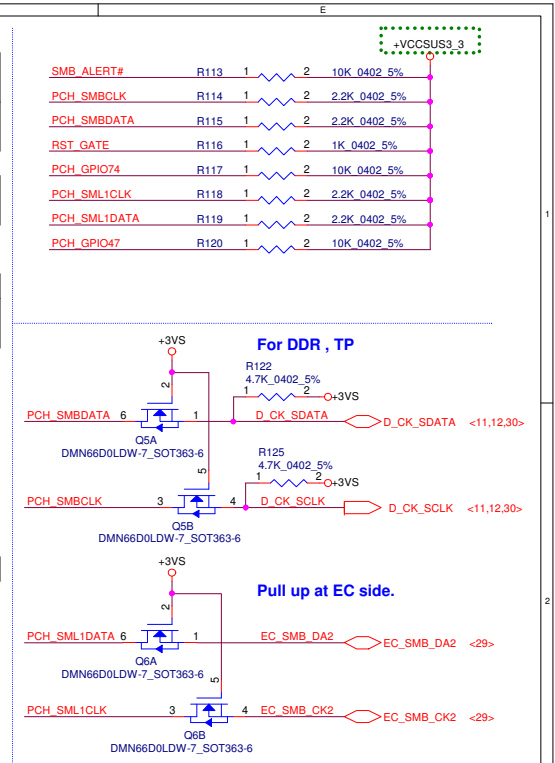
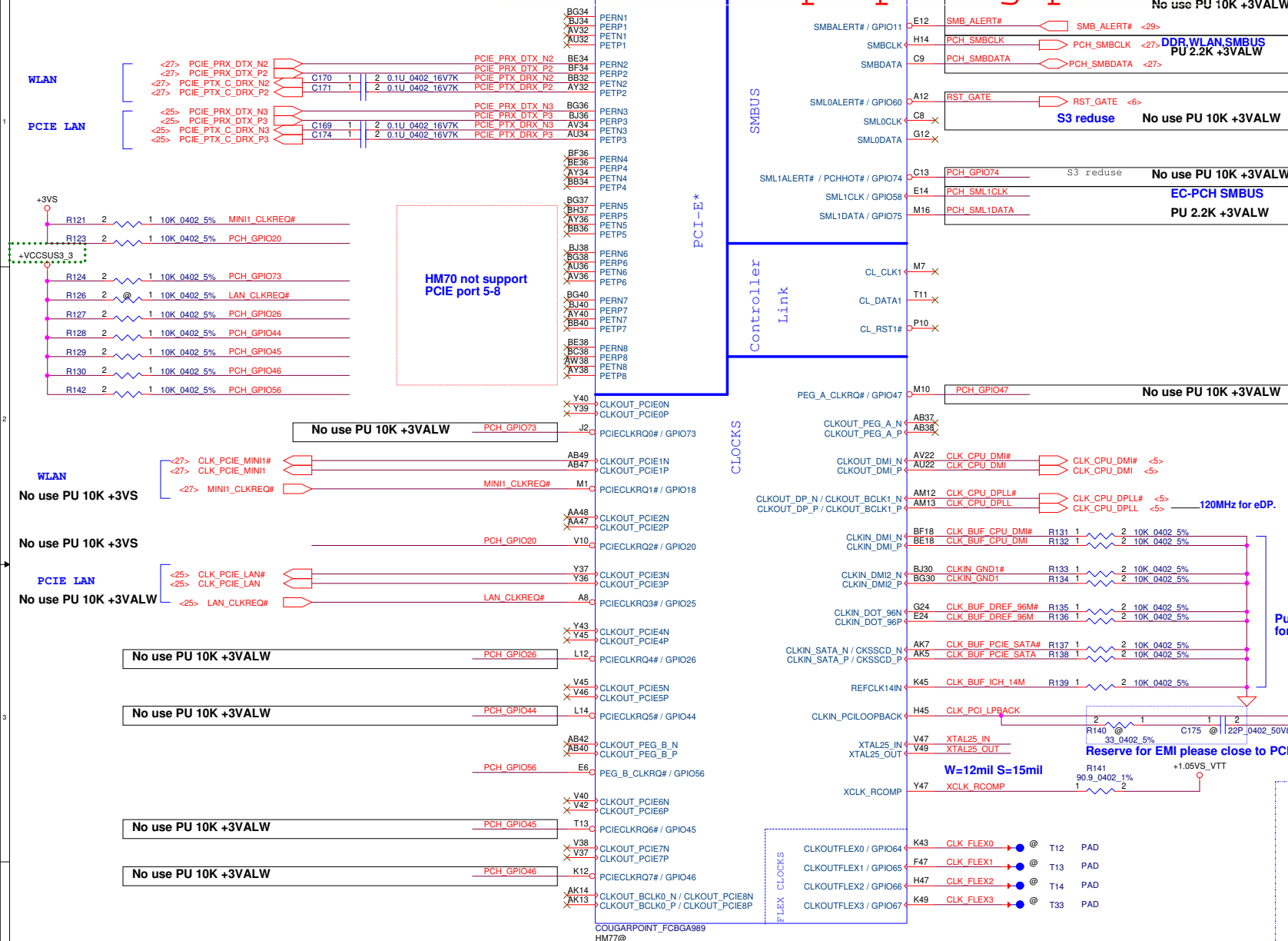
Channel B

<Address: SA1:SA0=10>
12/21 Modify

DIMM_2 Reverse H:4.0mm

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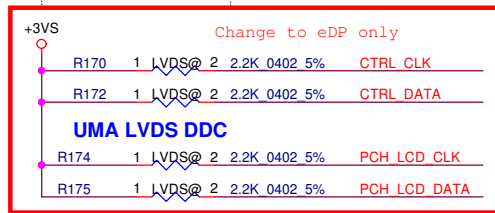


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UMA Panel Backlight ON/OFF

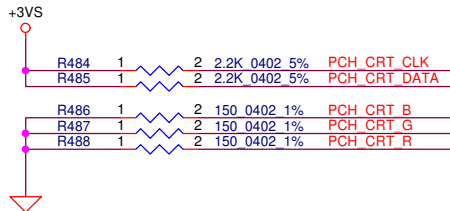
<29> ENBKL ← ENBKL R169 2 1 0.0402 5% IGPU BKLT EN

PD 100K
at EC side

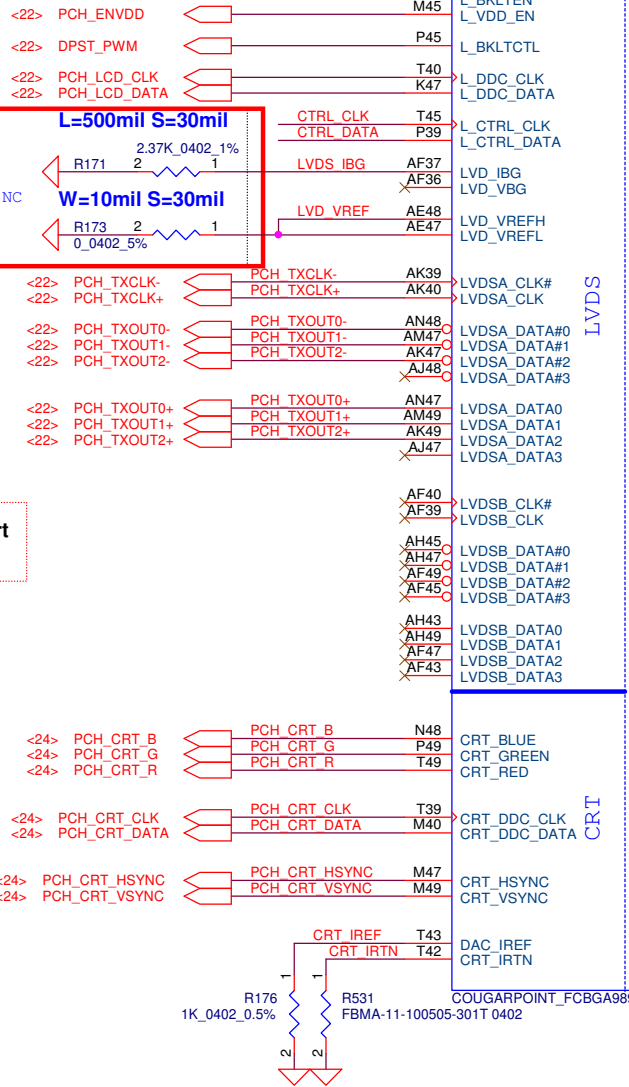


Check list1.5 P.60 disable Graphics
ALL Can NC
but DAC_IREF still need PD

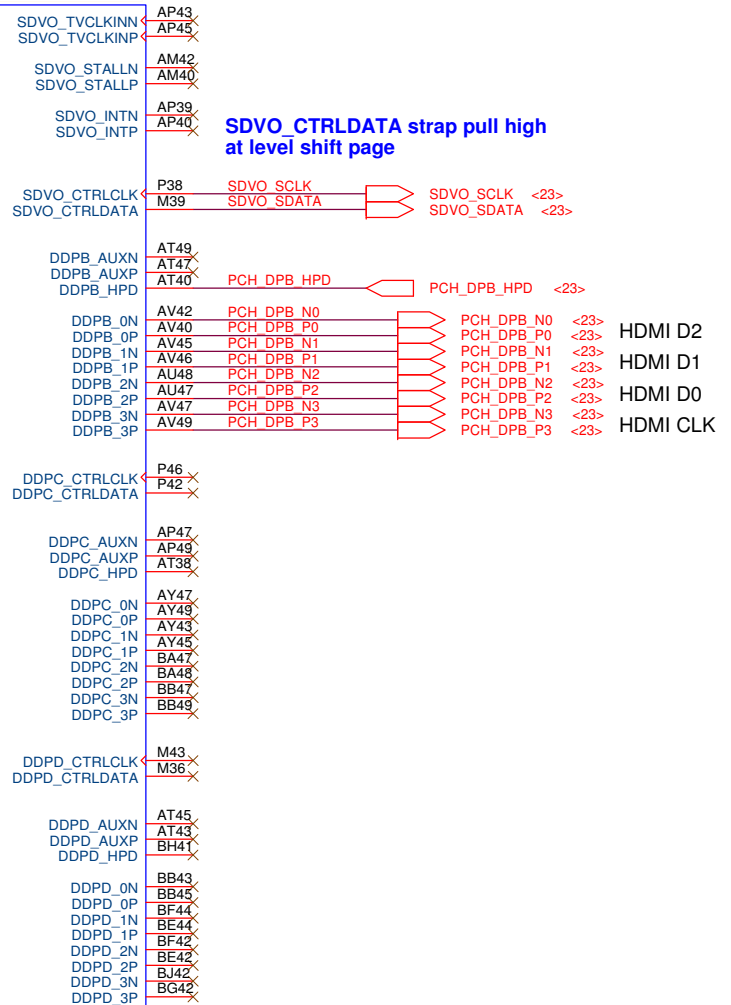
LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND



UM77 not support
LVDS/CRT



Digital Display Interface



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12/6 Add R469-R480

8.2K 0402 5% 2 1 R469 PCI_PIRQC#
 8.2K 0402 5% 2 1 R470 PCI_PIRQB#
 8.2K 0402 5% 2 1 R471 PCI_PIRQA#
 8.2K 0402 5% 2 1 R472 PCI_PIRQD#

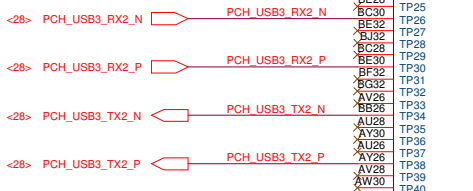
8.2K 0402 5% 2 1 R473 PCH_GPIO55
 8.2K 0402 5% 2 1 R474 PCH_GPIO53
 8.2K 0402 5% 2 1 R475 PCH_GPIO52
 8.2K 0402 5% 2 1 R476 PCH_GPIO5

8.2K 0402 5% 2 1 R477 PCH_GPIO51
 8.2K 0402 5% 2 1 R478 PCH_GPIO2
 8.2K 0402 5% 2 1 R480 PCH_GPIO4

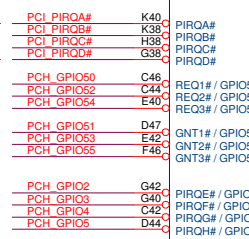
8.2K 0402 5% 2 1 R523 PCH_GPIO3
 10K 0402 5% 2 1 R180 PCH_GPIO54



USB3.0

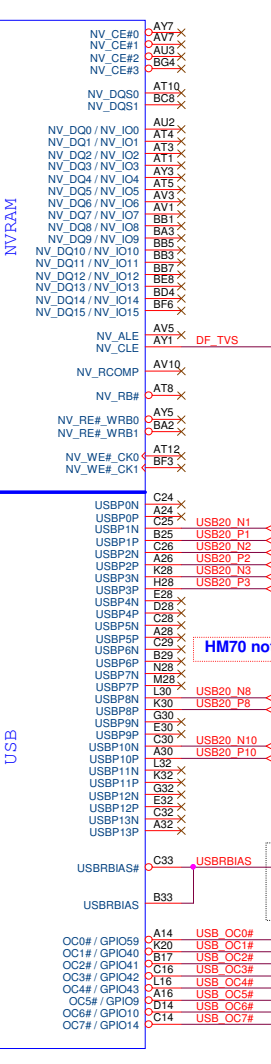
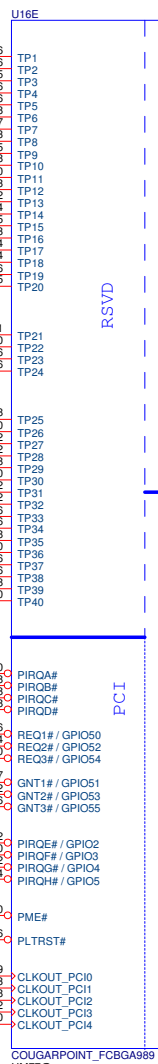
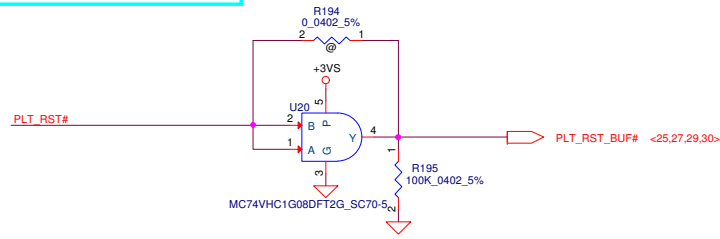
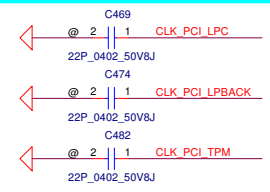


PCI Interrupt Requests



<14> CLK_PCI_LPBACK <29> CLK_PCI_LPC <30> CLK_PCI_TPM

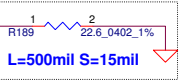
11/30 Add (EMI request)



HM70 not support USB2.0 for port 4-7 & 12 & 13

Mini Card (WLAN)

CMOS Camera (LVDS)



L=500mil S=15mil

DMI, FDI Termination Voltage

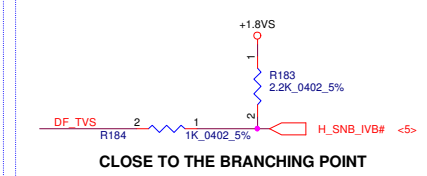
DF_TVS	Set to Vcc when HIGH
	Set to Vss when LOW

*Note: 457511 Rev 1.3-p.20

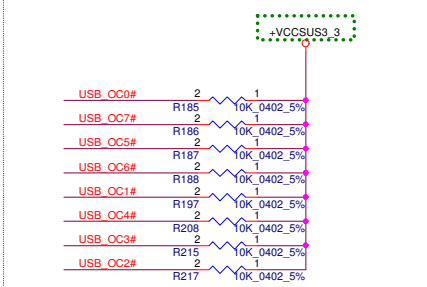
HR CPU NC

HR&CR co-layer CPU PU

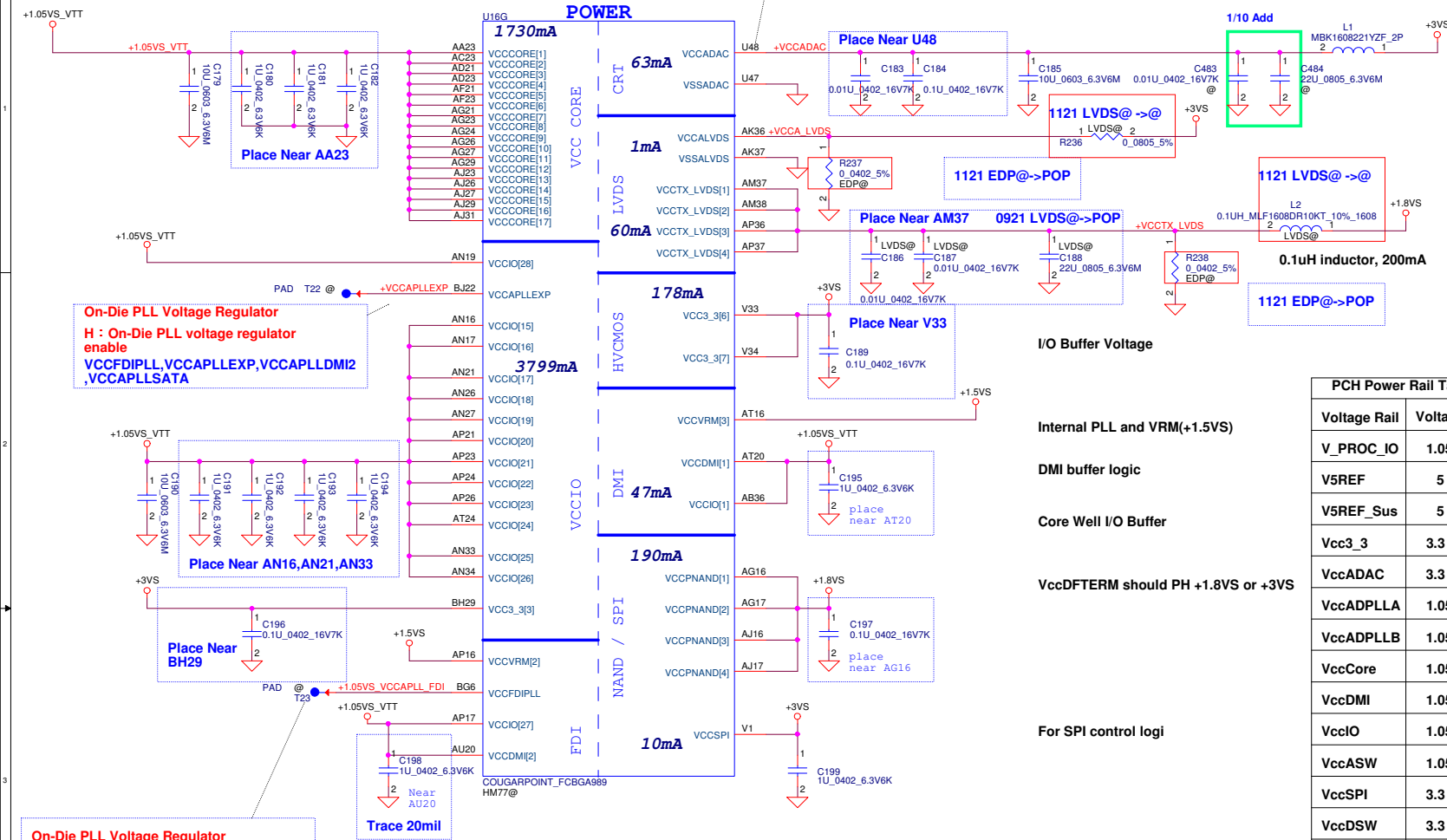
CR Check list P.89 PU 2.2K series 1K



CLOSE TO THE BRANCHING POINT

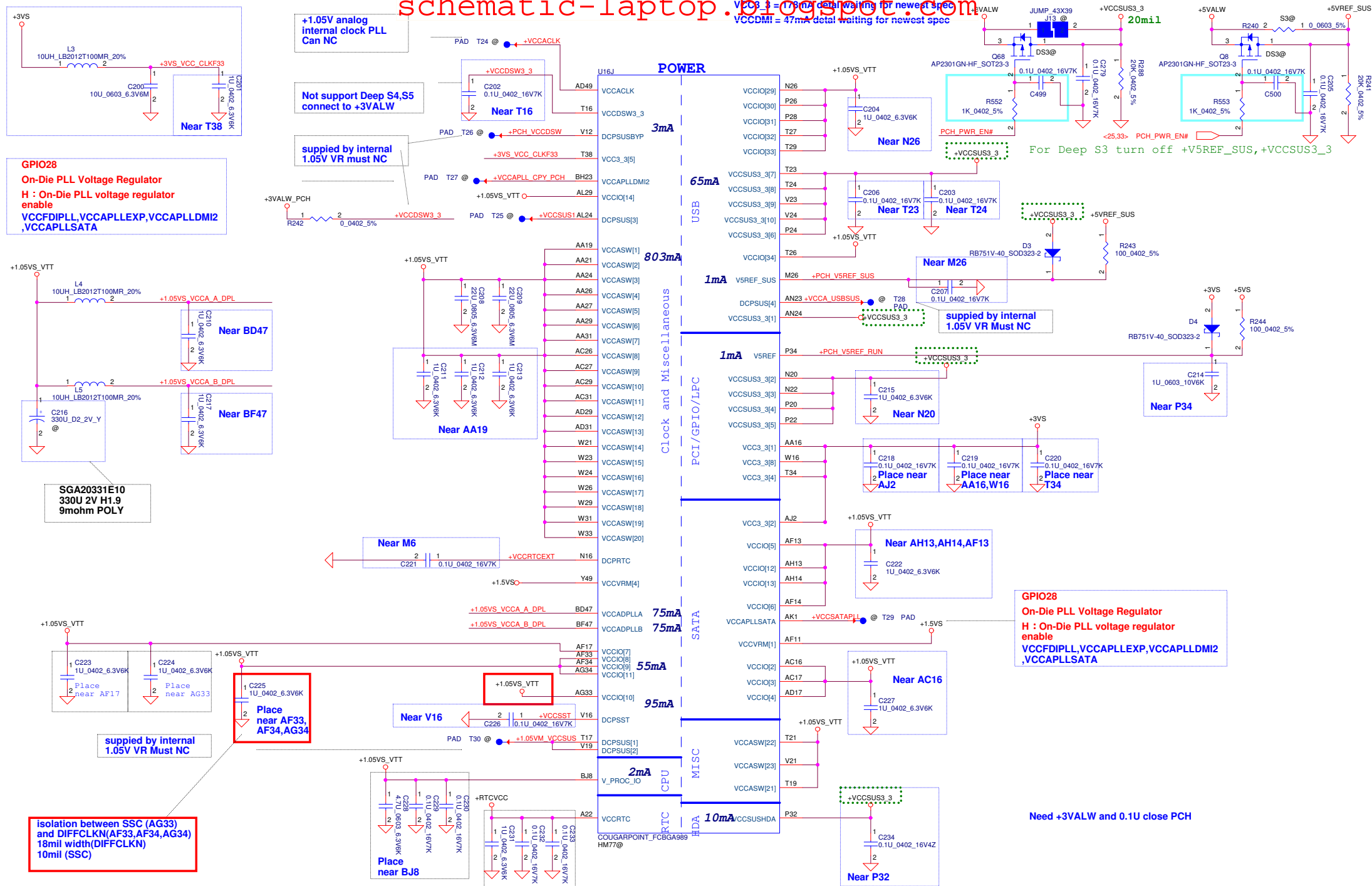


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				Document Number	Rev
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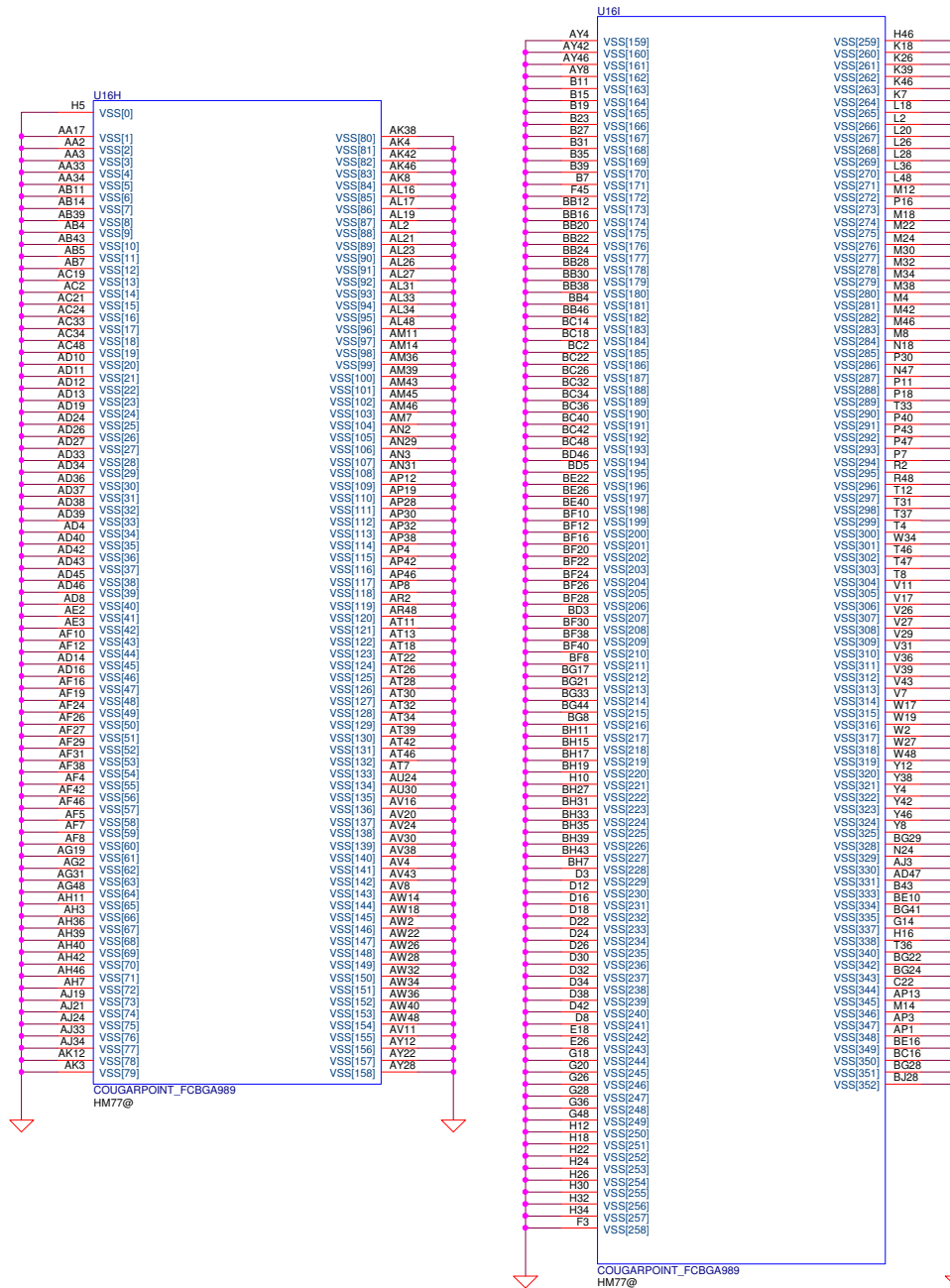


PCH Power Rail Table			
Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.002	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.178	I/O Buffer Voltage
VccADAC	3.3	0.063	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.075	Display PLL A power
VccADPLLB	1.05	0.075	Display PLL B power
VccCore	1.05	1.73	Internal Logic Voltage
VccDMI	1.05	0.047	DMI Buffer Voltage
VccIO	1.05	3.799	Core Well I/O buffers
VccASW	1.05	0.803	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.01	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8v power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.065	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

VCC3_3 = 178mA detal waiting for newest speed



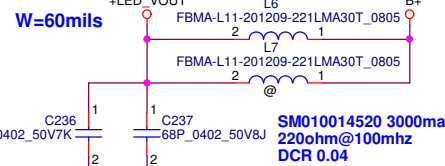
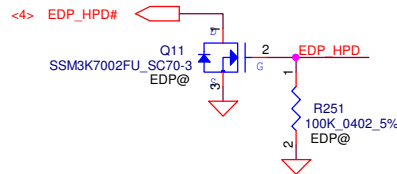
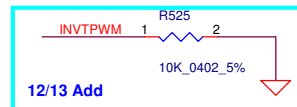
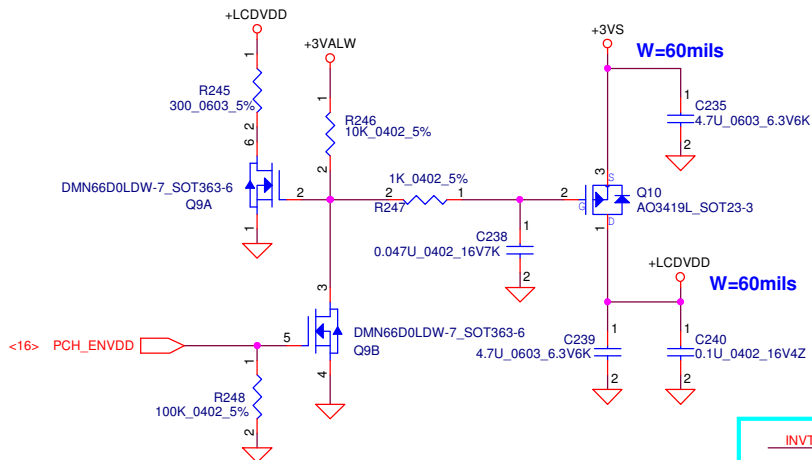
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Date: Friday, April 20, 2012				Sheet 20 of 45	



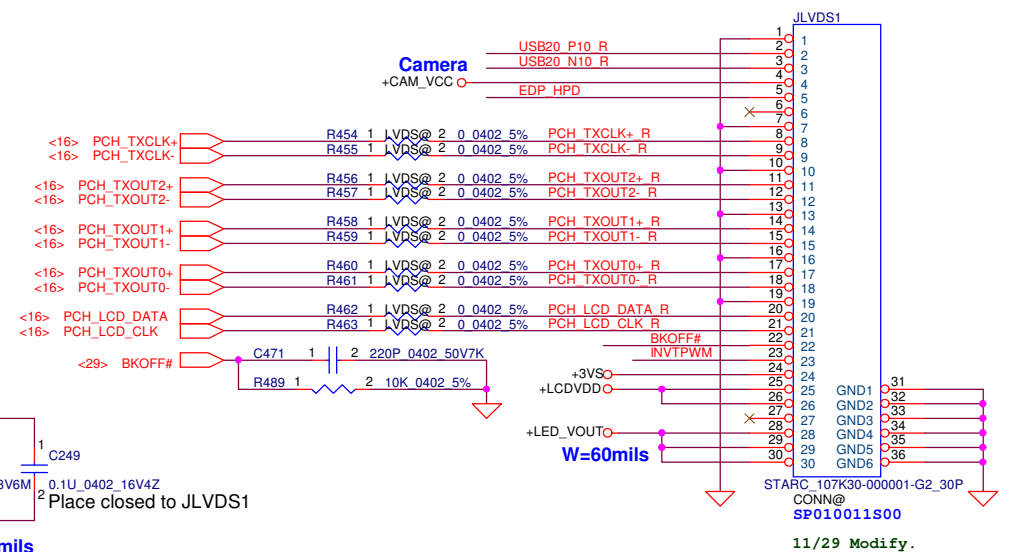
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LCD POWER CIRCUIT

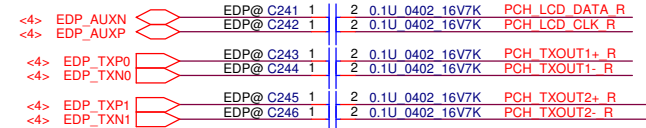
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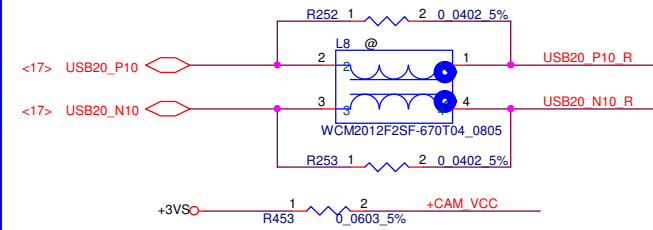
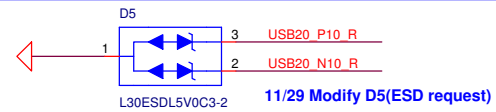
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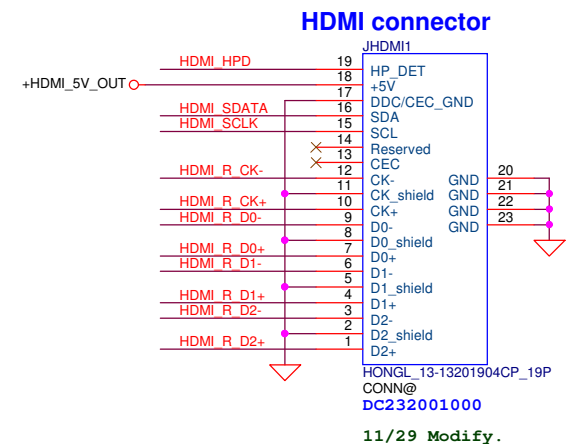
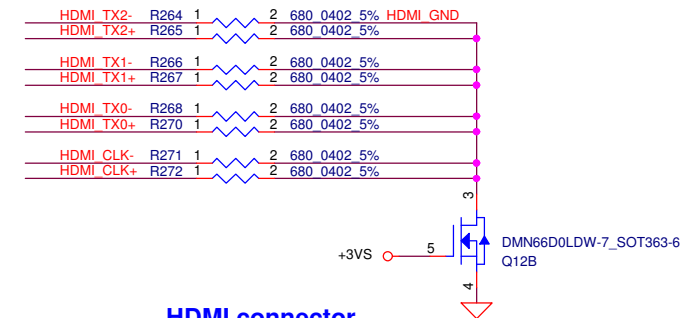
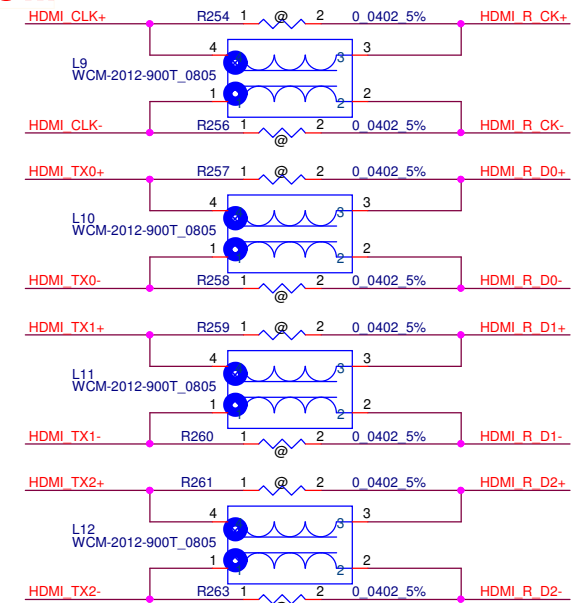
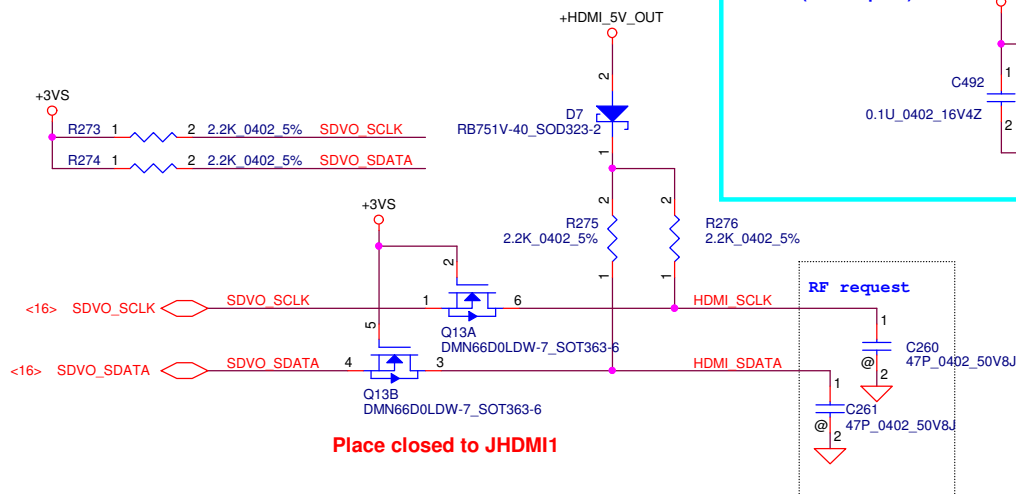
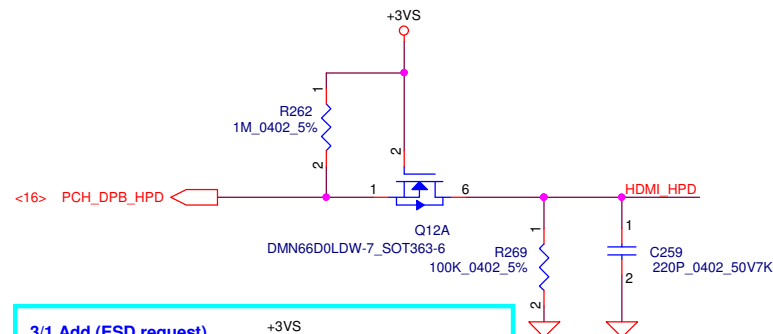
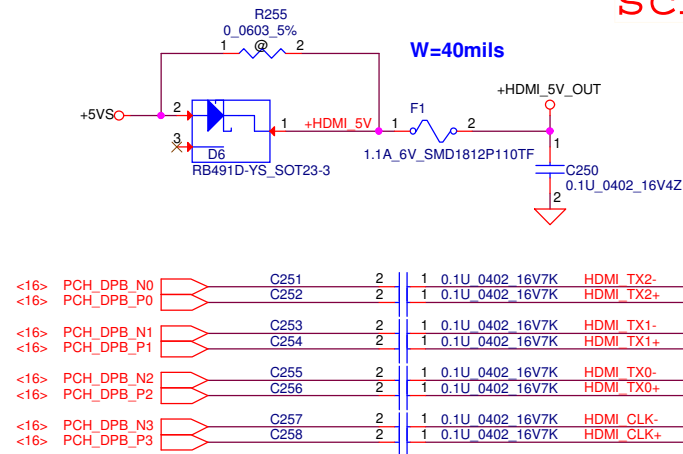
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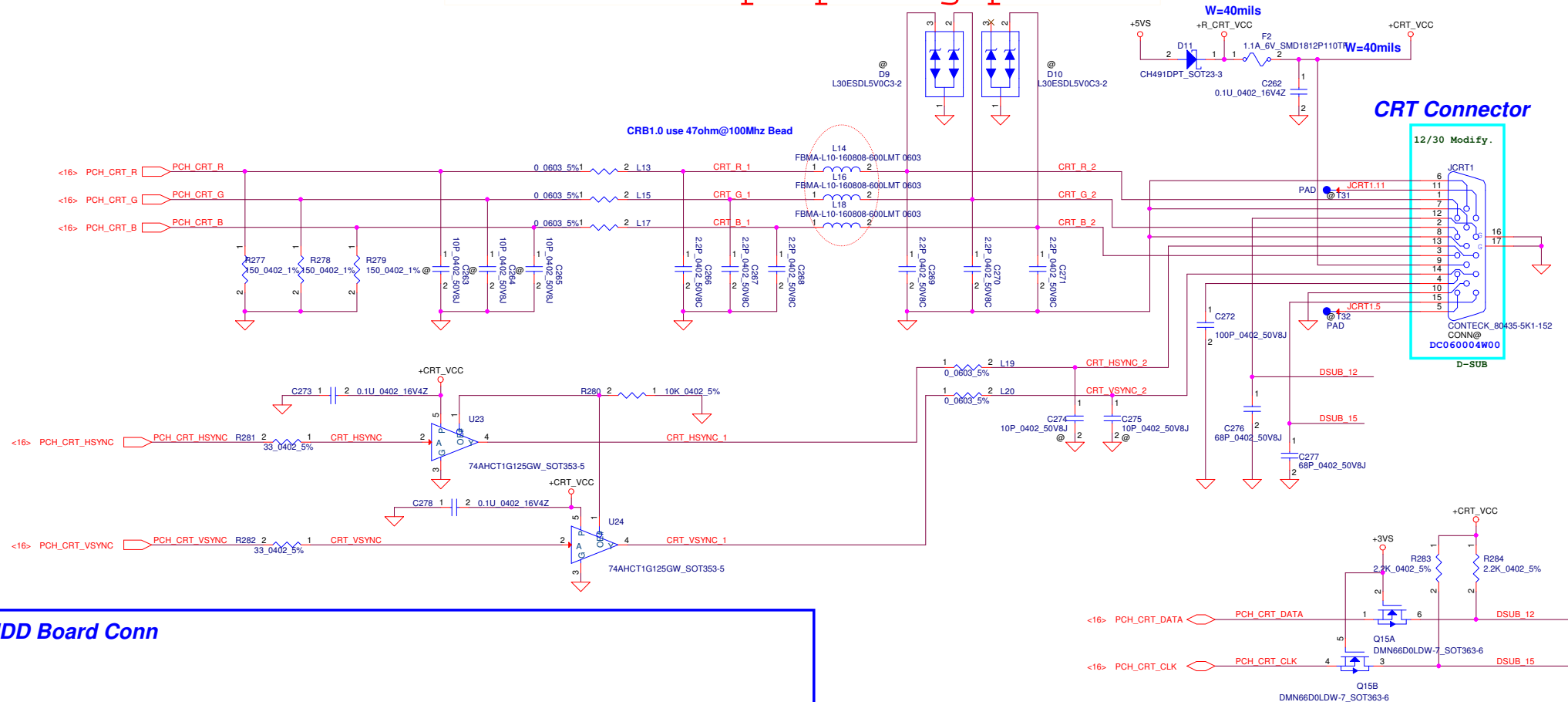
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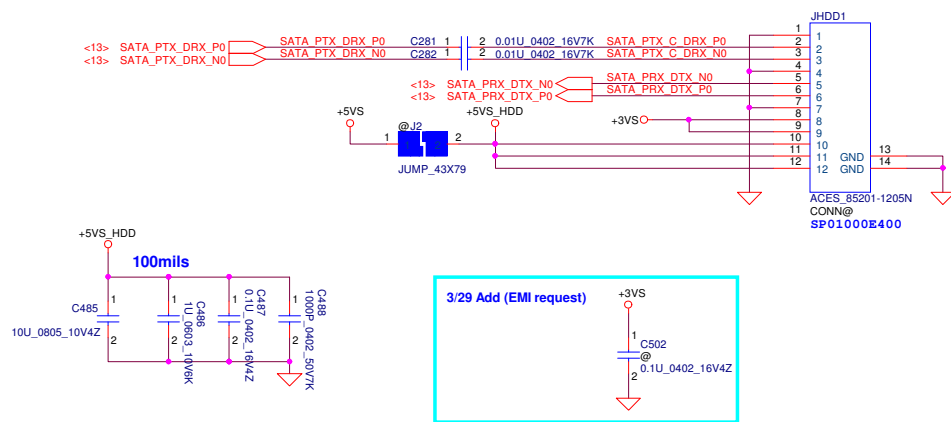
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										Rev 1.0	
										Date: Friday, April 20, 2012	
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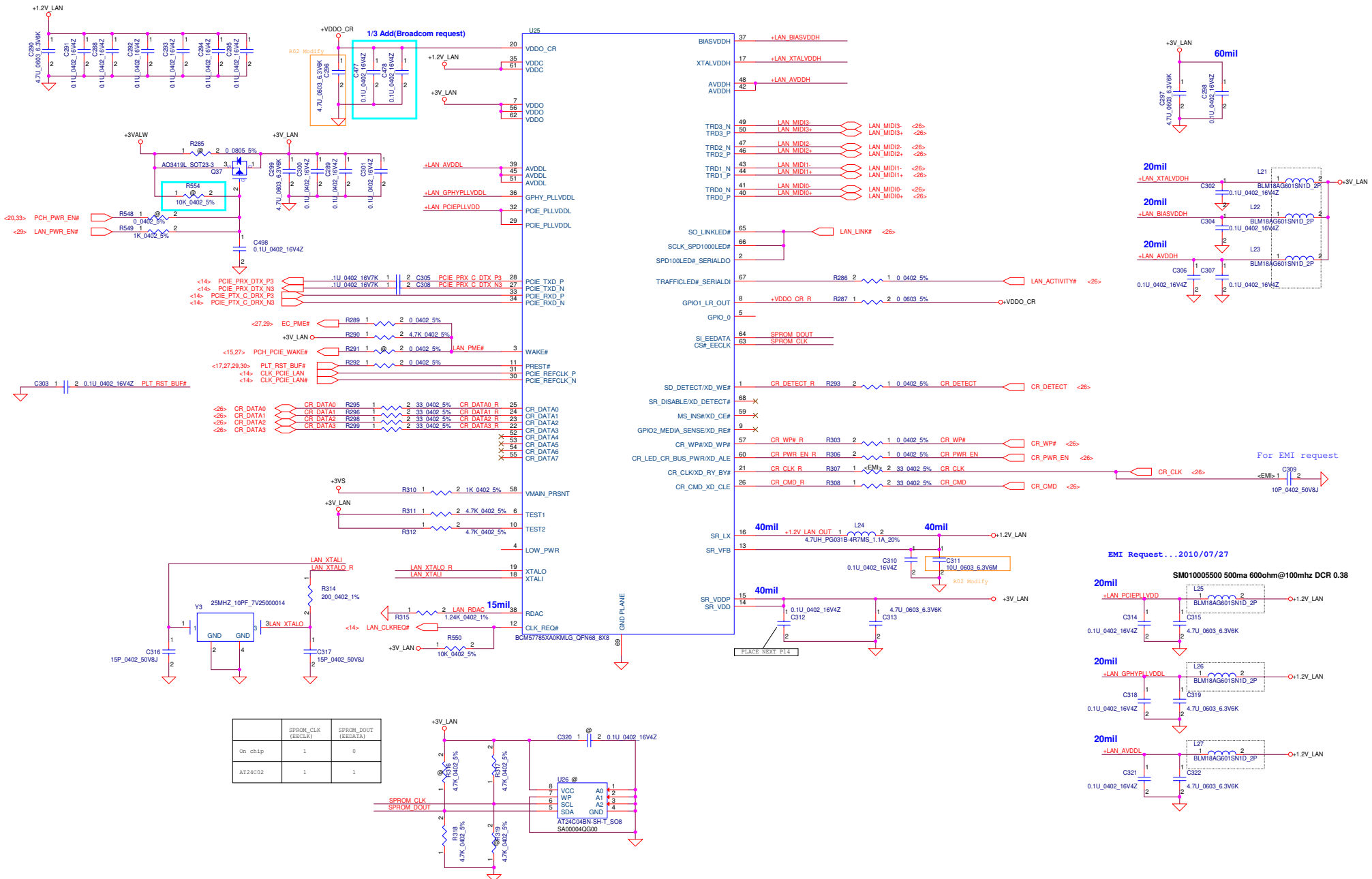
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Size		Document Number		Rev	
Custom		Q1VZC M/B LA-8941P Schematic		1.0	
Date:		Friday, April 20, 2012		Sheet 23 of 45	



HDD Board Conn

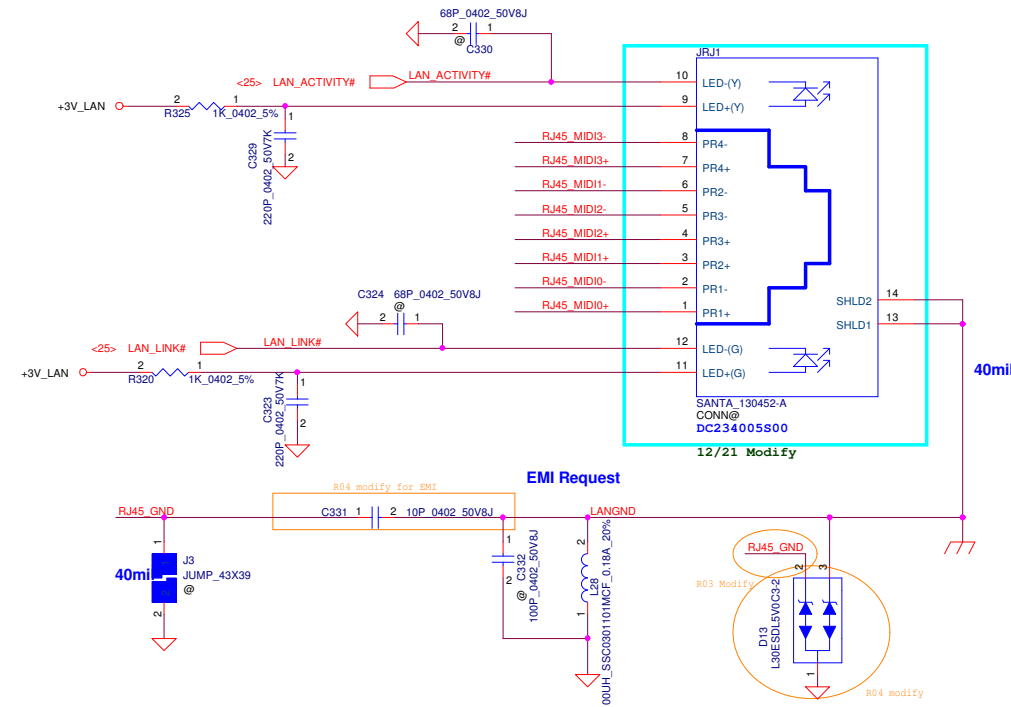
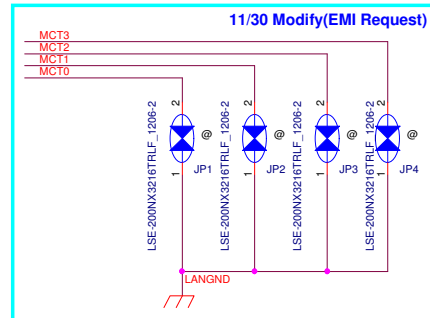
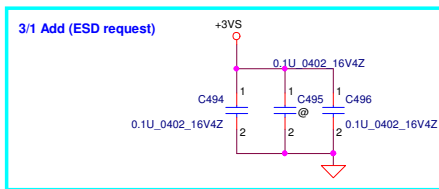
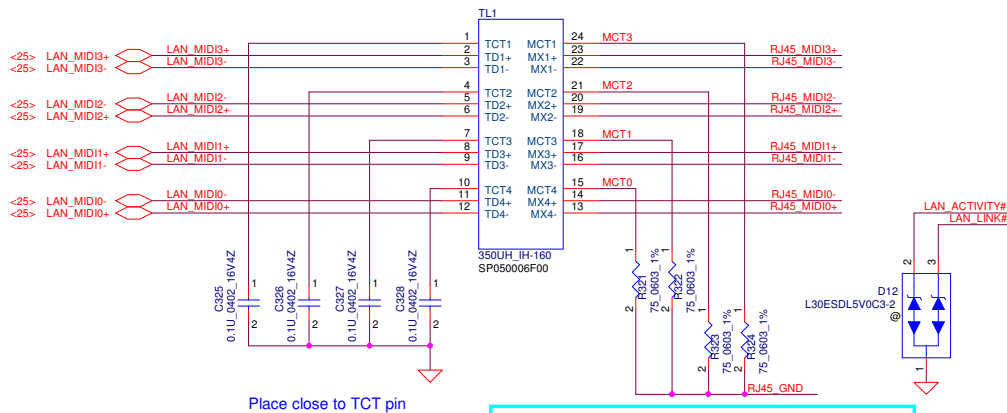


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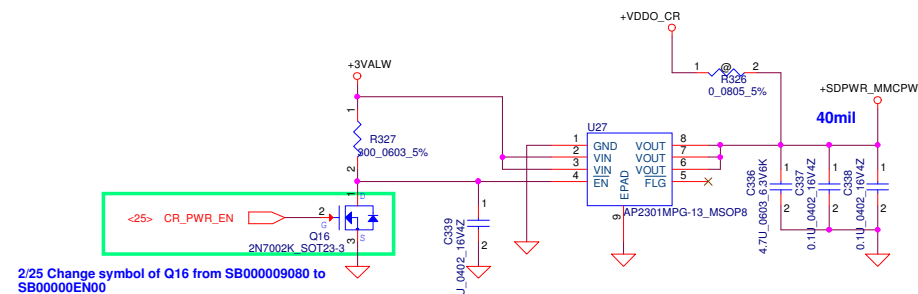
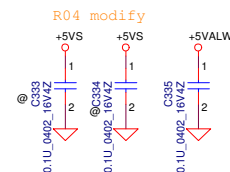
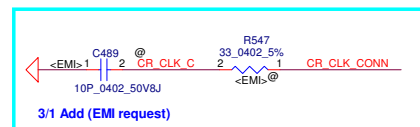
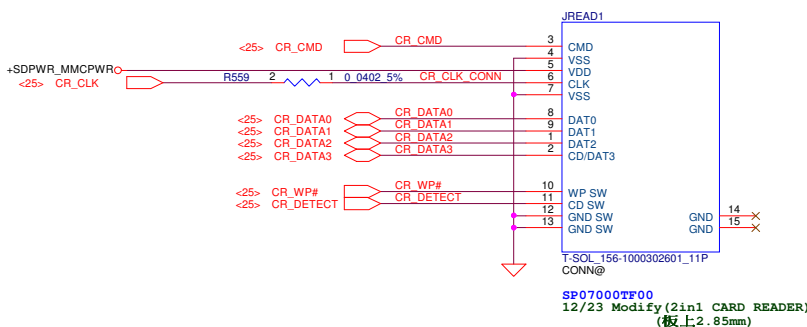


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C474, C475 and D14
ME interfere, do not pop!!

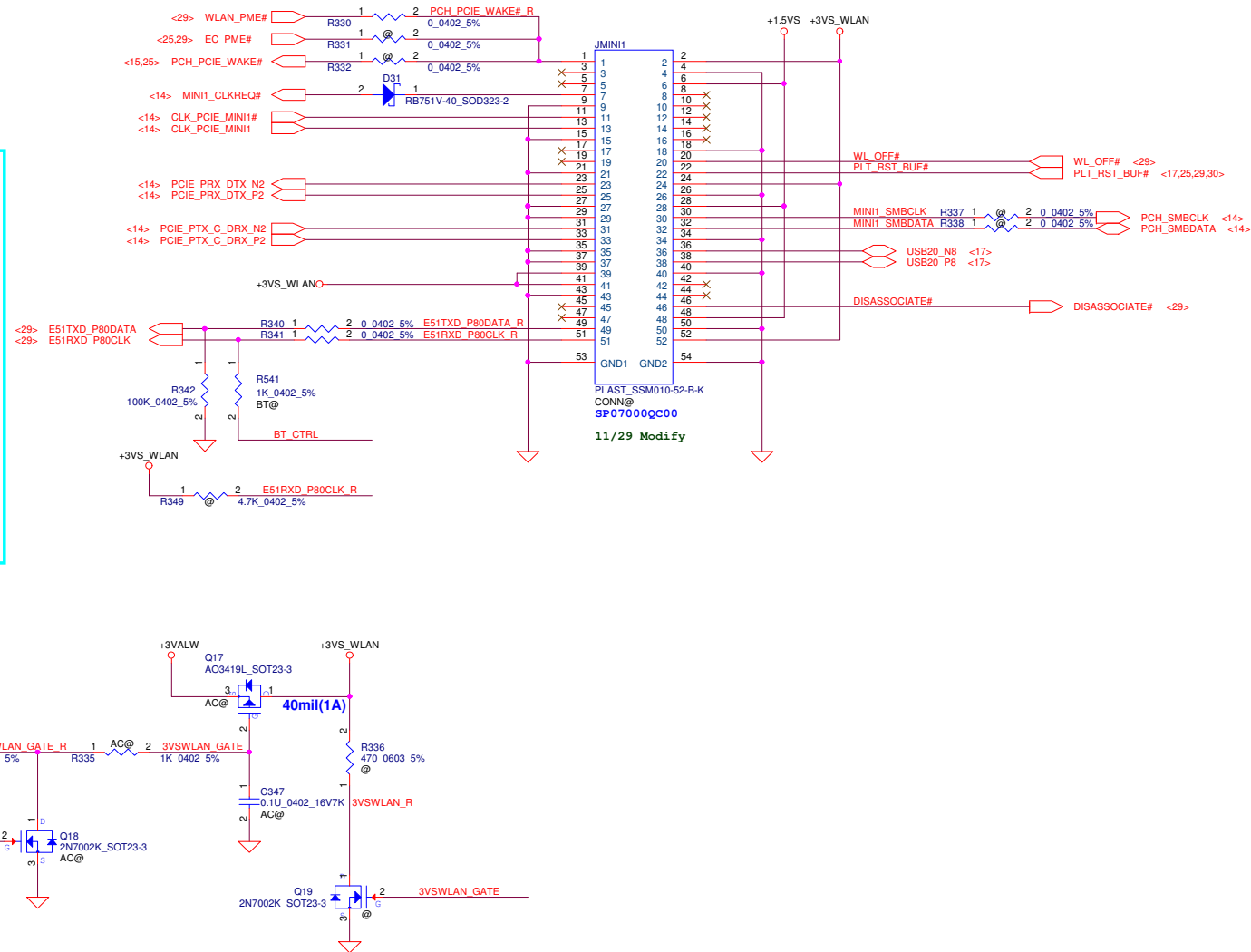


Card Reader Connector



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			Date		Friday, April 20, 2012	
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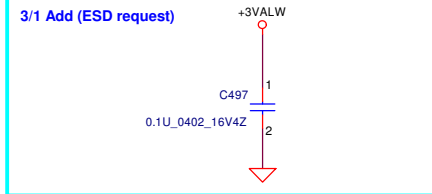
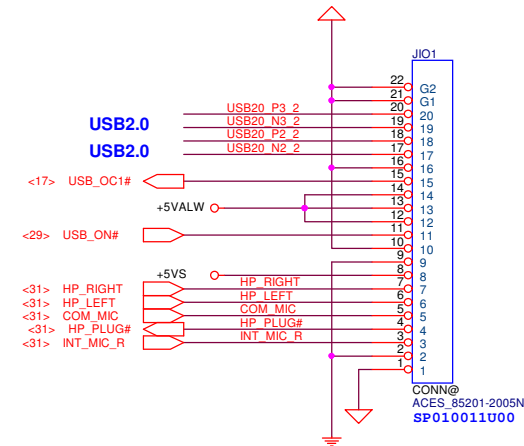
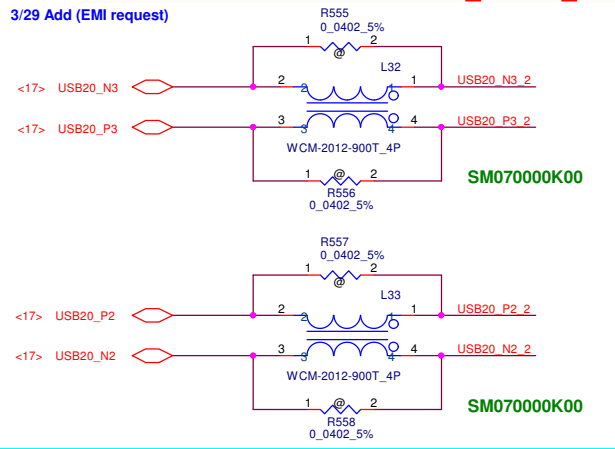
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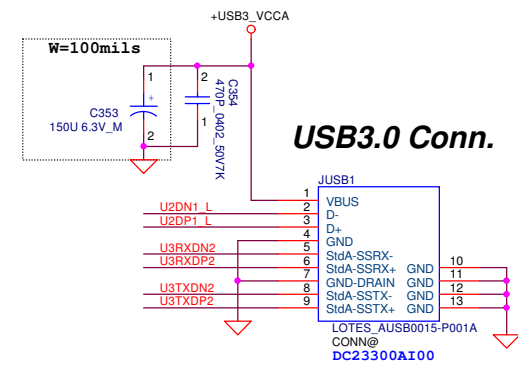
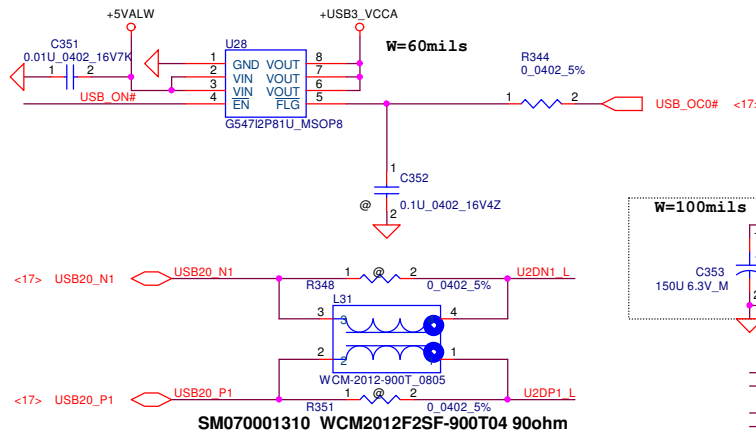
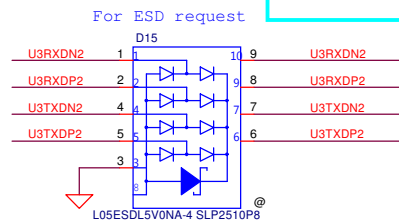
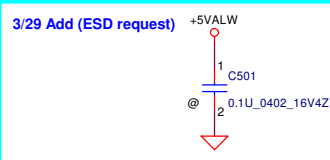
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IO Board

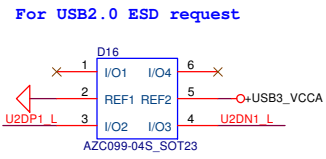
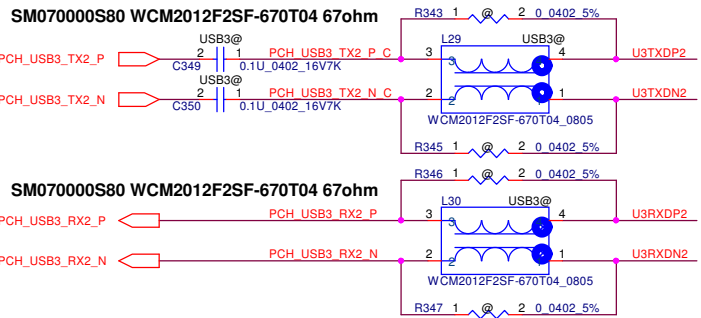
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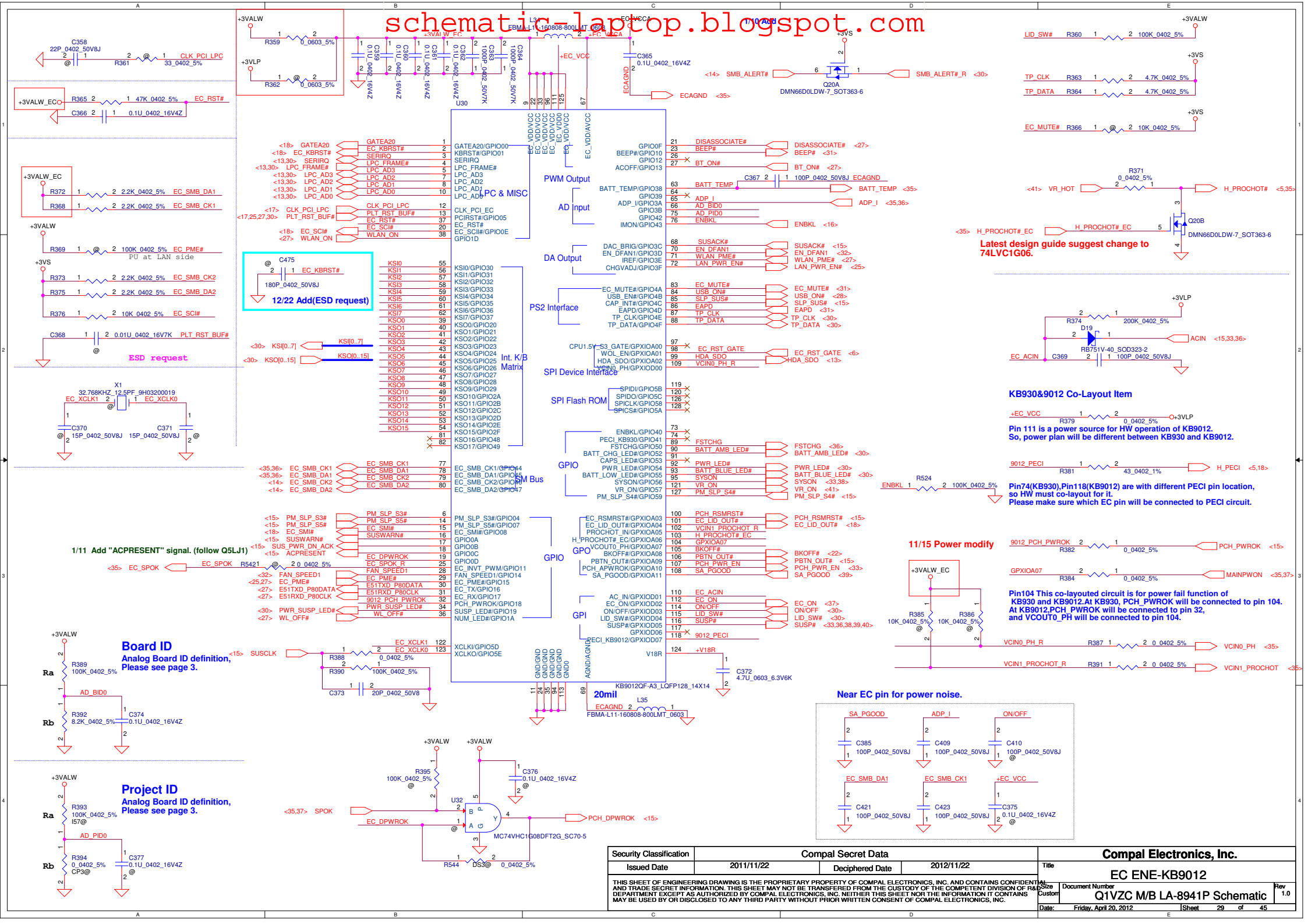
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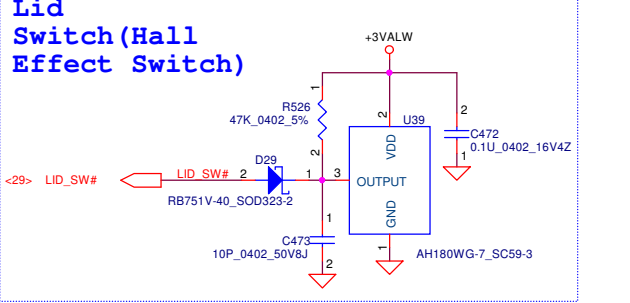
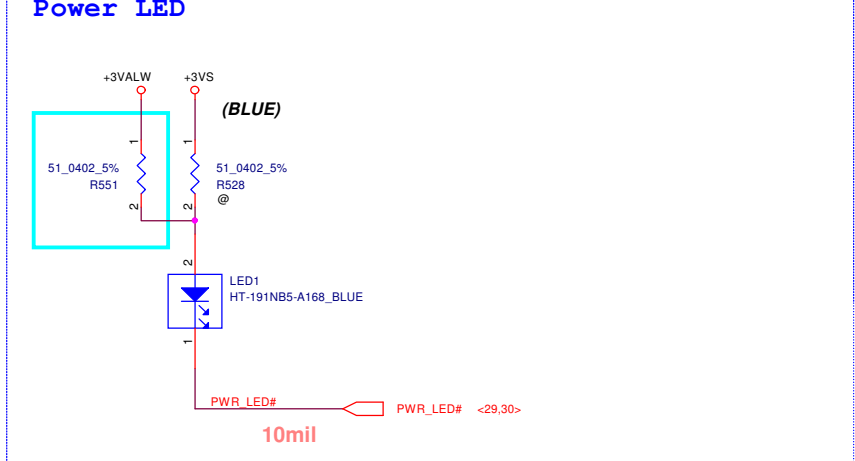
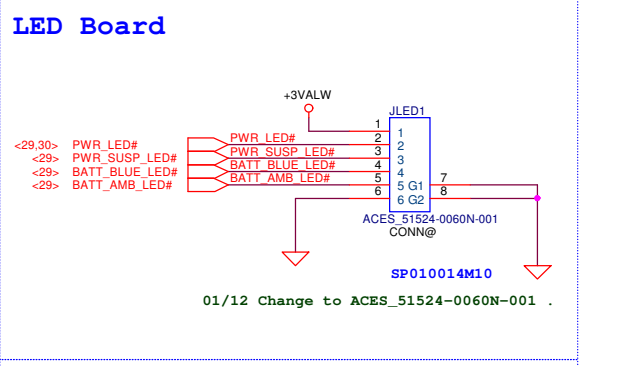
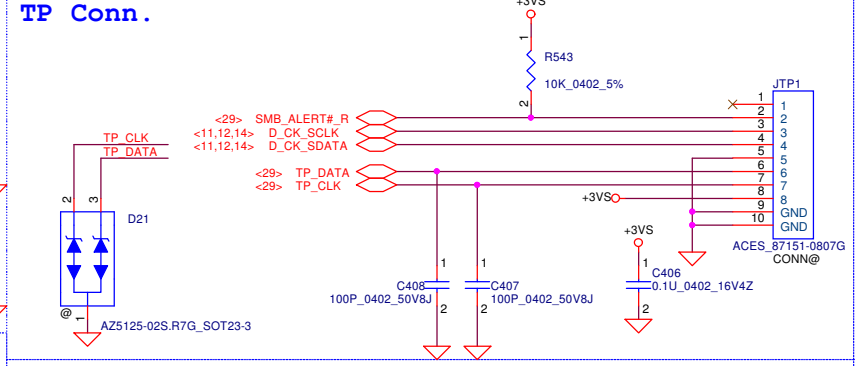
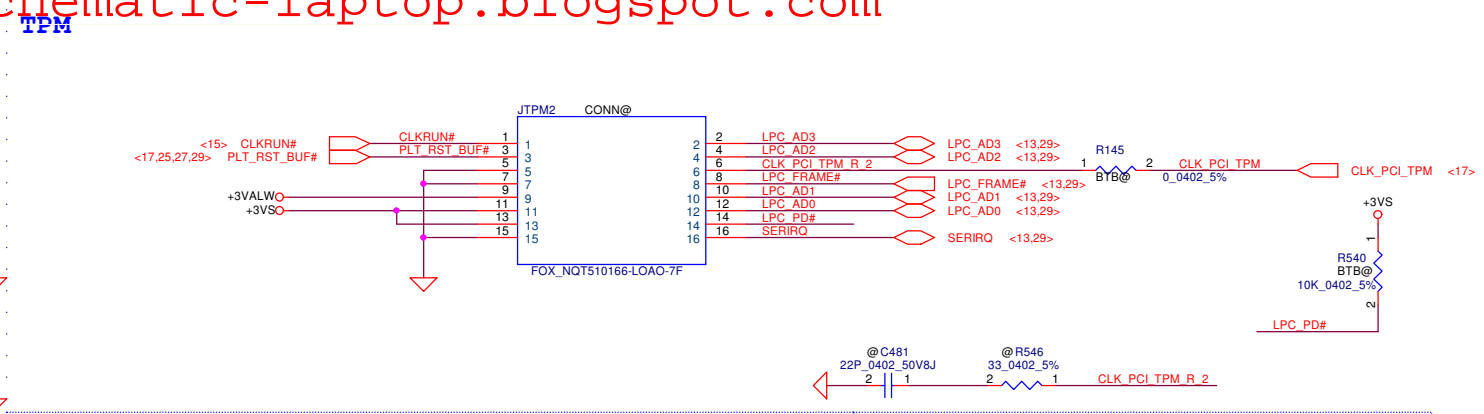
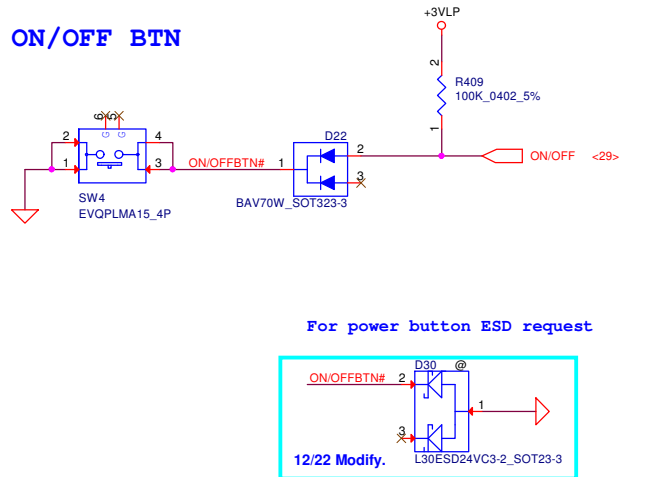
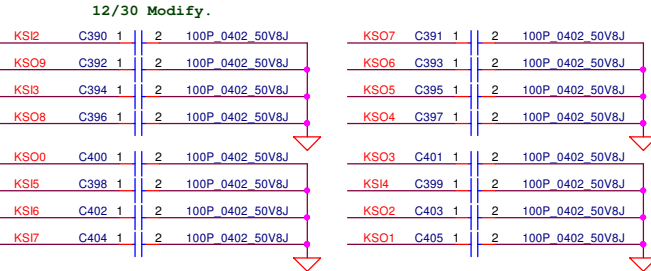
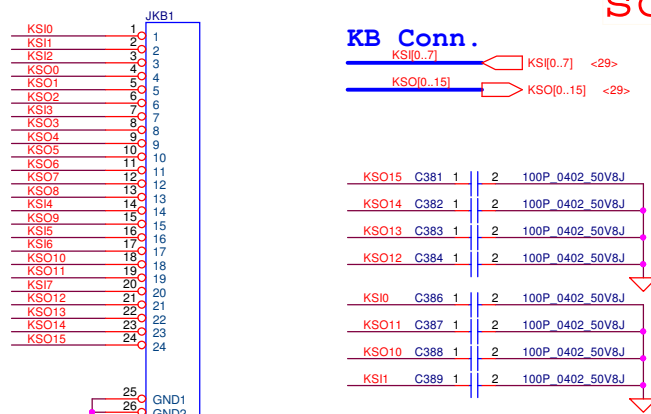


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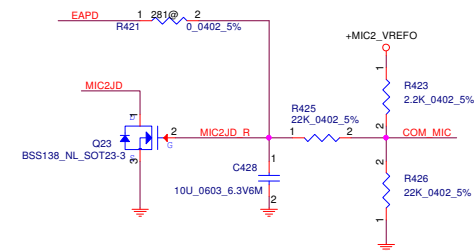
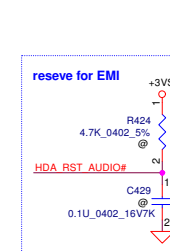
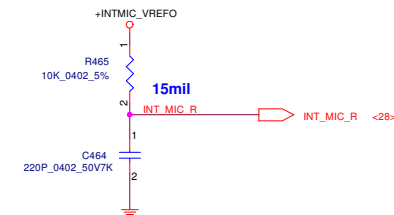
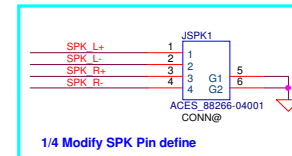
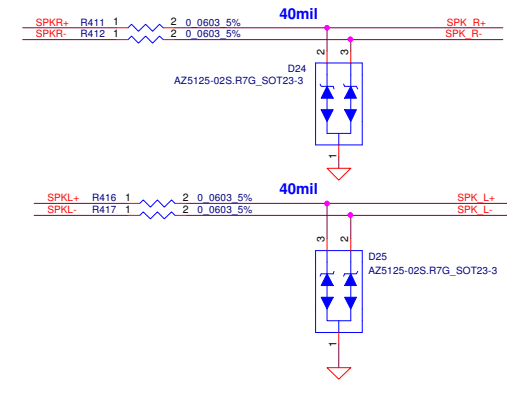


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						Custom		Q1VZC M/B LA-8941P Schematic				1.0	
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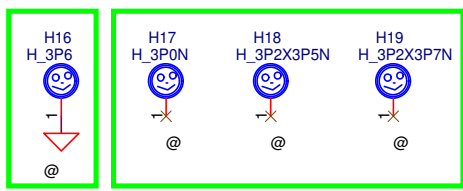
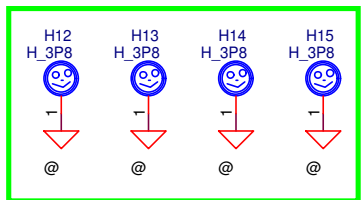
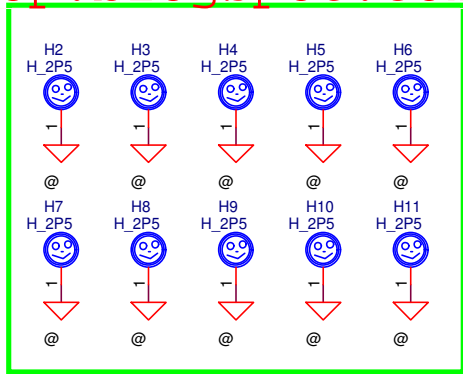
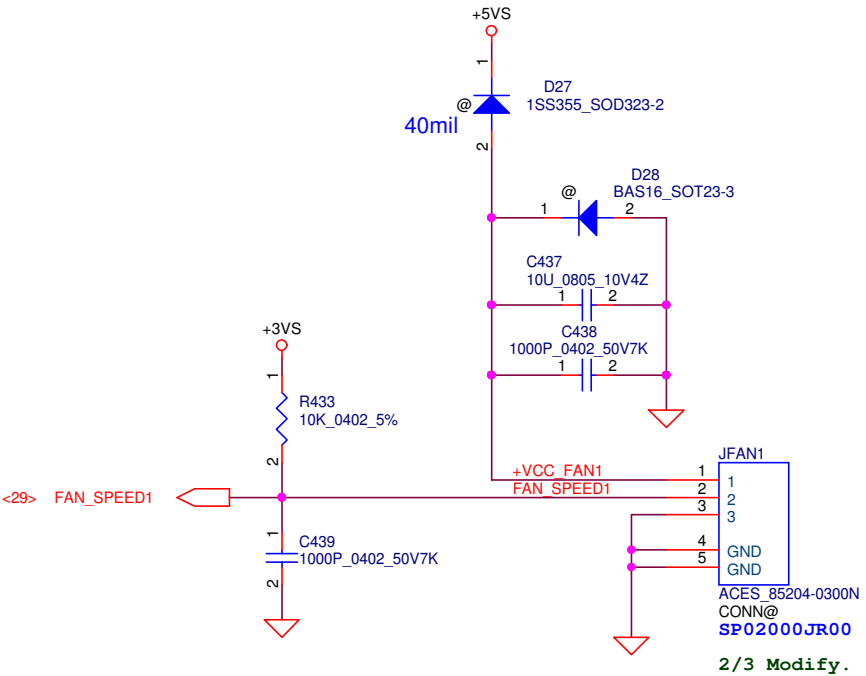


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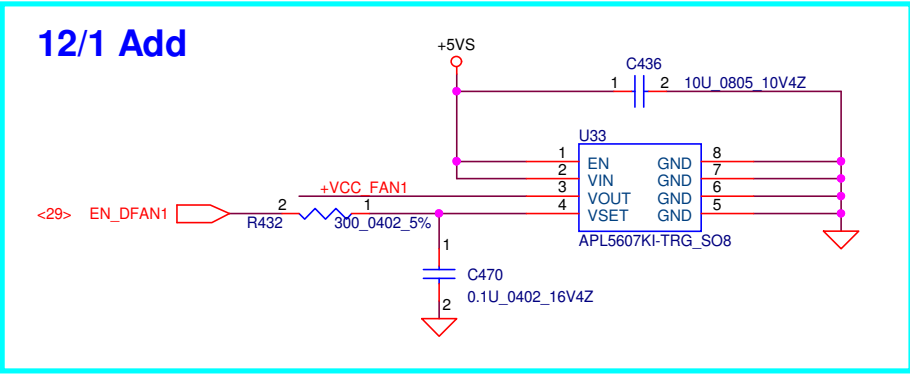
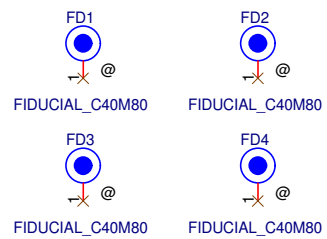


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FAN1 Conn

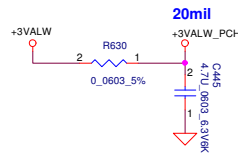
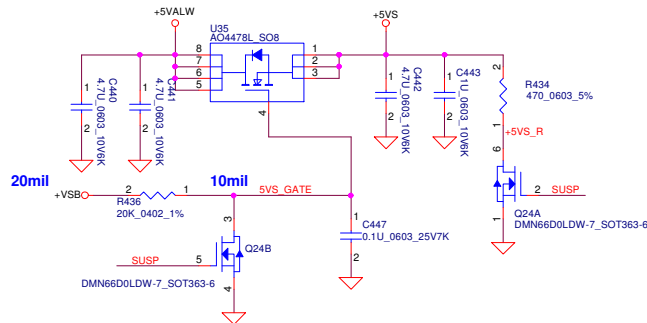


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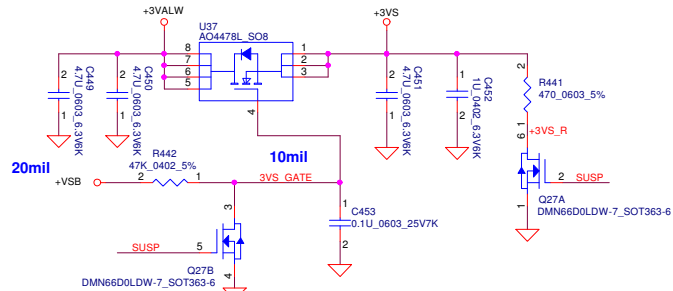


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				Date:	Rev 1.0
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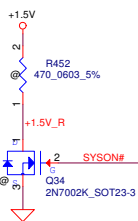
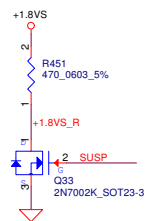
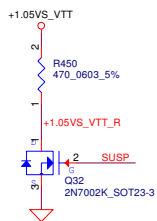
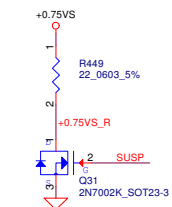
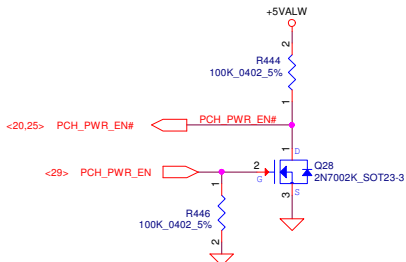
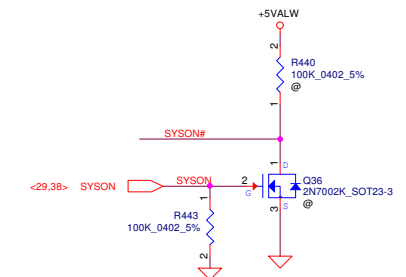
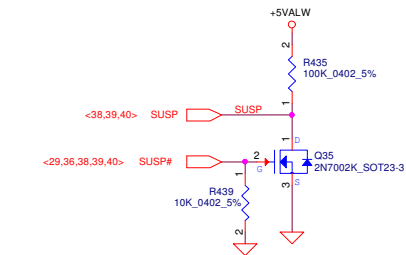
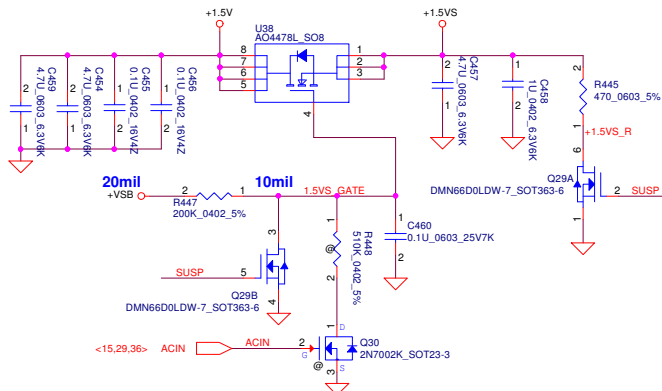
+5VALW TO +5VS

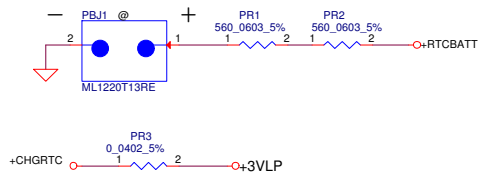
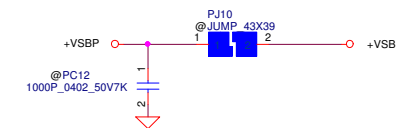
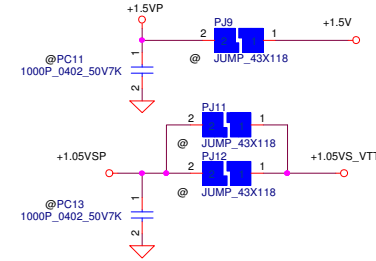
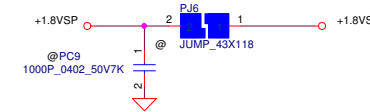
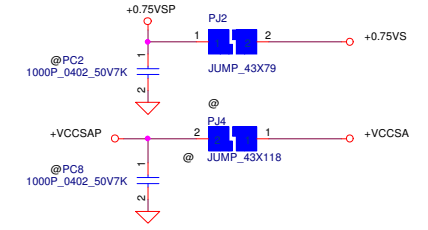
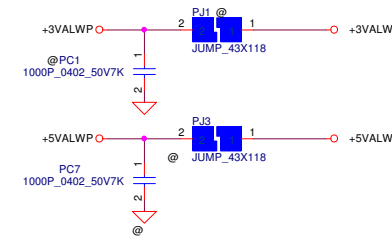
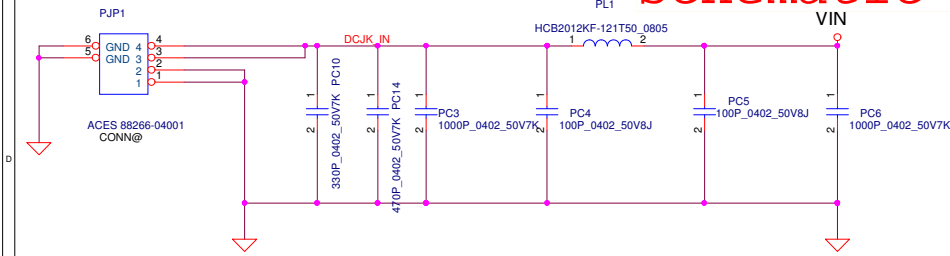


+3VALW TO +3VS

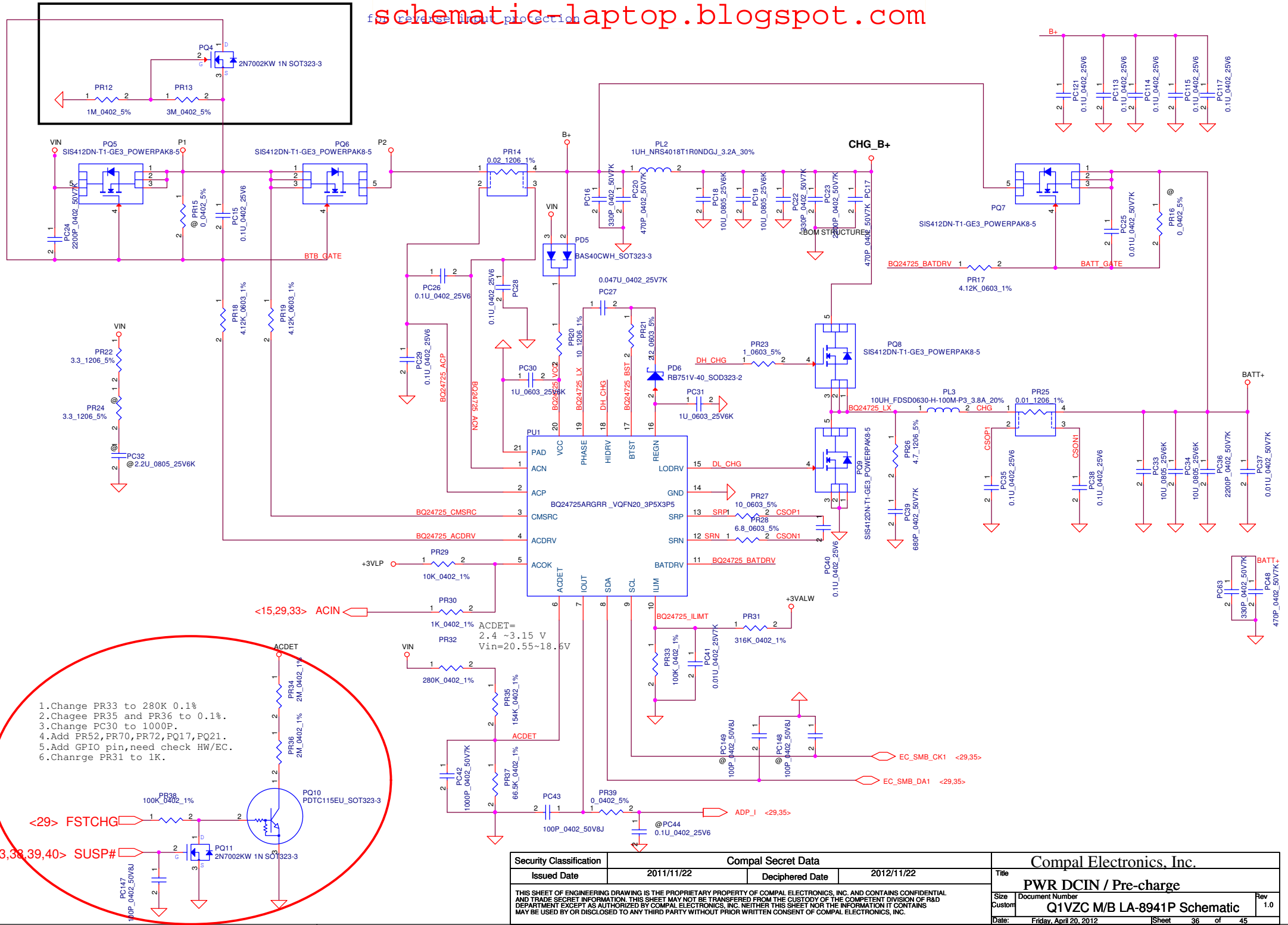


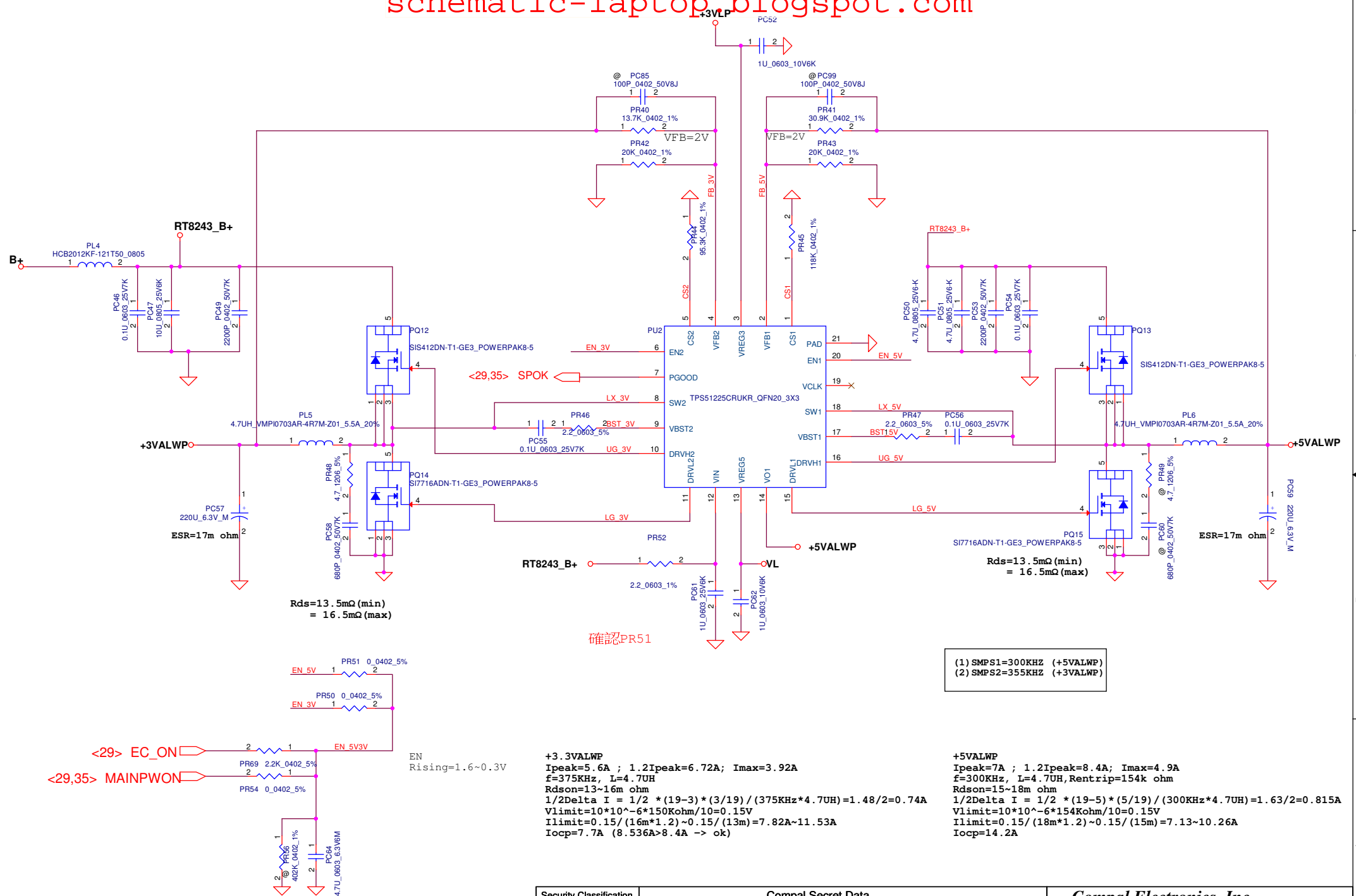
+1.5V to +1.5VS



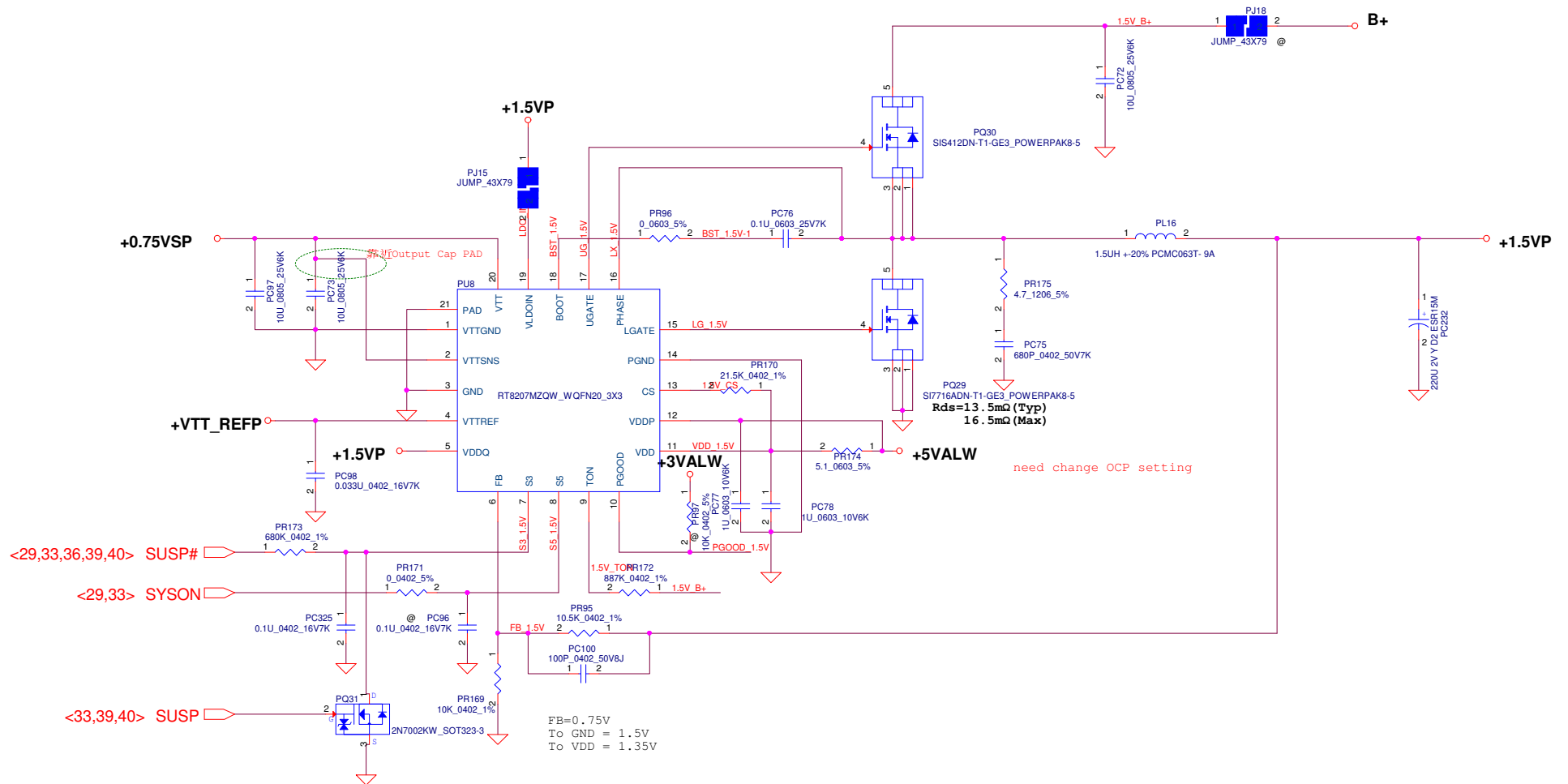


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<Vo=1.5V> VFB=0.75V
 $V = 0.75 * (1 + 10K / 10.5K) = 1.52V$
 $F_{sw} = 286K \text{ to } 200KHz$

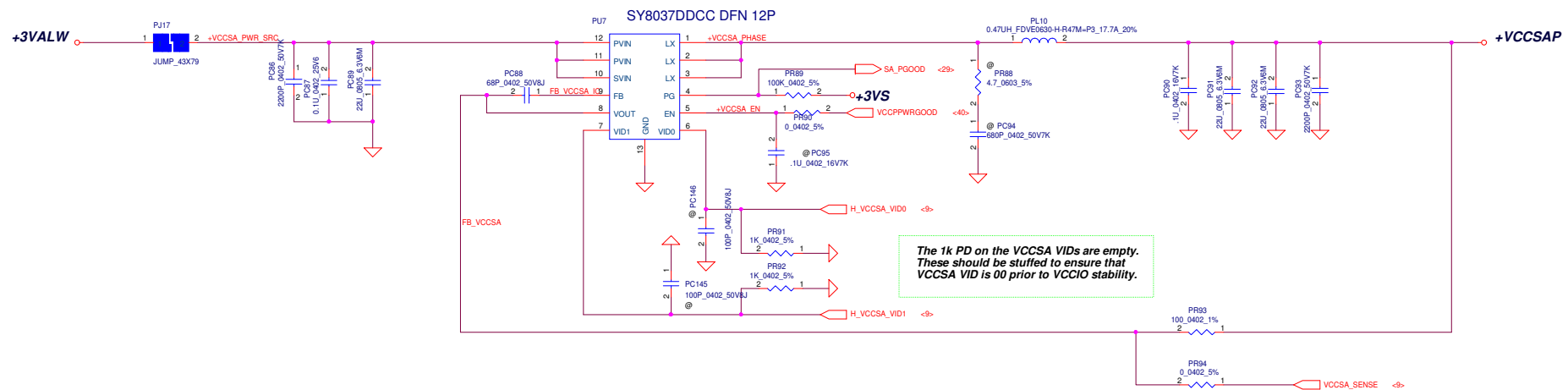
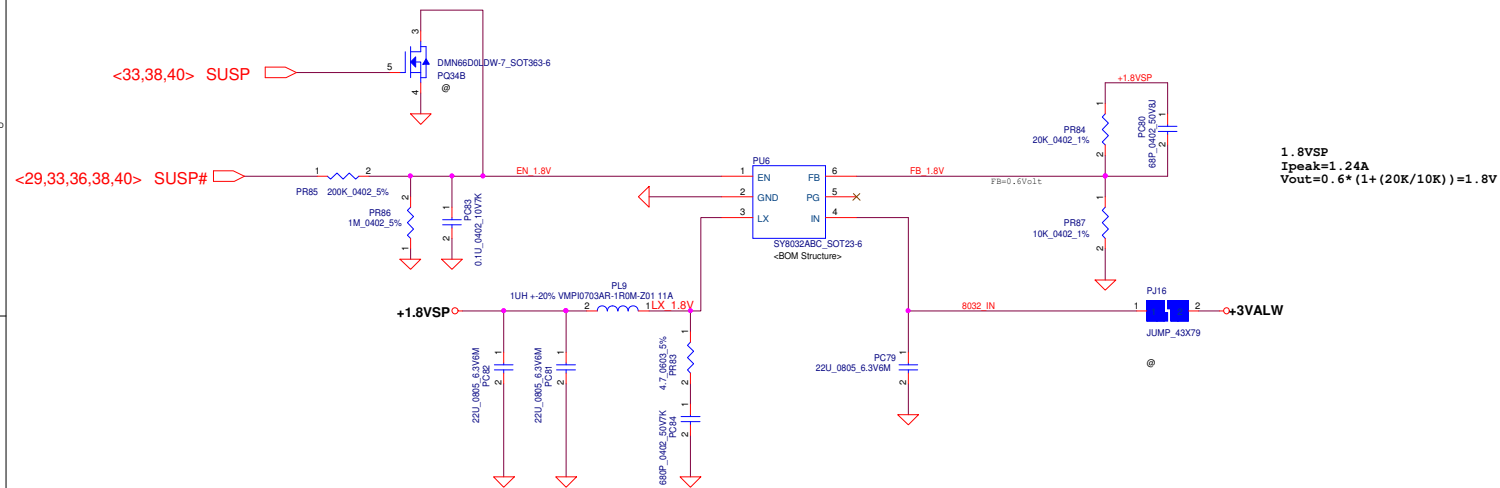
Cout ESR=17m ohm Rds(on)(max)=16.5 mohm Rds(on)(typ)=13.5 mohm.
 $I_{peak} = 12A, I_{max} = 8.4A, I_{ocp} = 14.4A$

$\Delta I = ((V_{in} - V_o) * (V_o / V_{in})) / (L * F_{sw}) = 2.195A$
 $\Rightarrow 1/2 \Delta I = 1.099A$

$I_{ocpmax} = ((21.5K * 11uA) / 0.0135) + 0.5 \Delta I = A$
 $I_{ocpmin} = ((21.5K * 9uA) / 0.0165) + 0.5 \Delta I = 15.6A$

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off



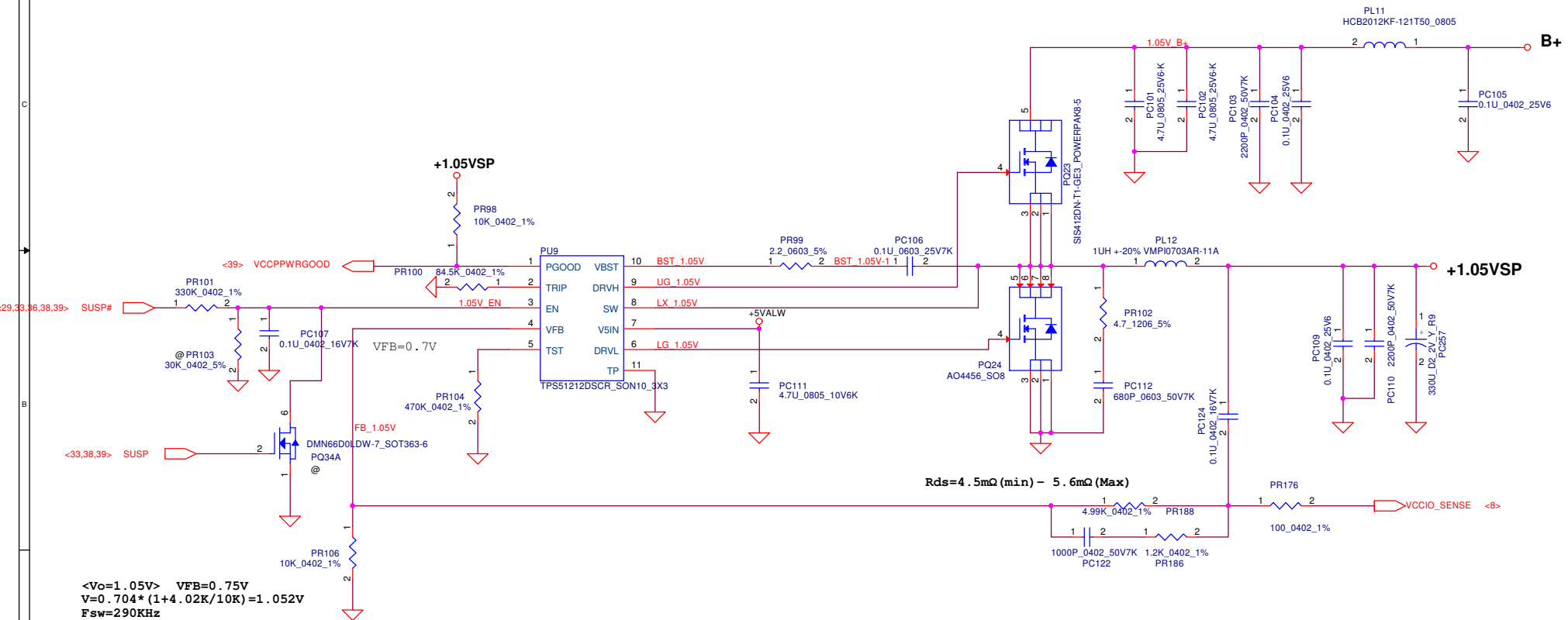
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

```
+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
```

VID [0]	VID[1]	VCCSA Vout (ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

output voltage adjustable network

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Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=15.6A, Imax=10.92A, Iocp=18.72A

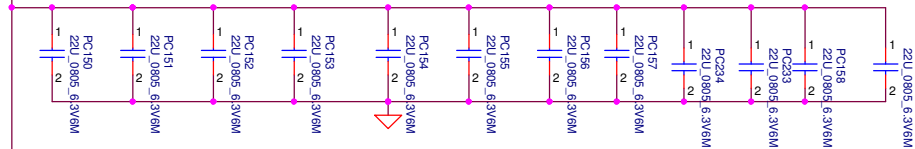
$$\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * F_{sw}) = 2.06A$$

```
Iocpmax=(15K*11uA)/0.0045)+1.665A=23.54A
Iocpmin=(15K*9uA)/(0.0056*1.3))+1.665A=19A
Iocp=A
```

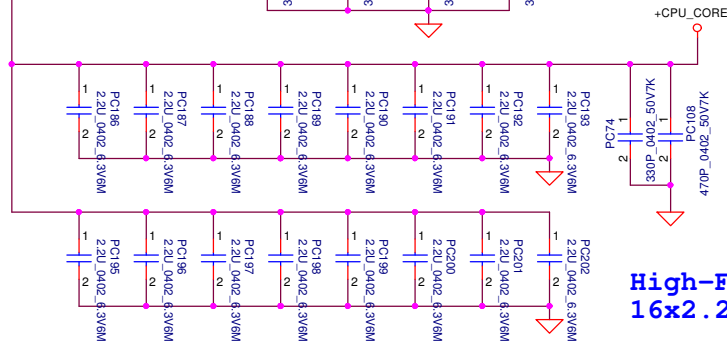
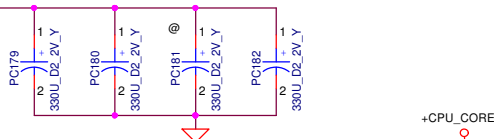
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CR PDDG Rev 0.95

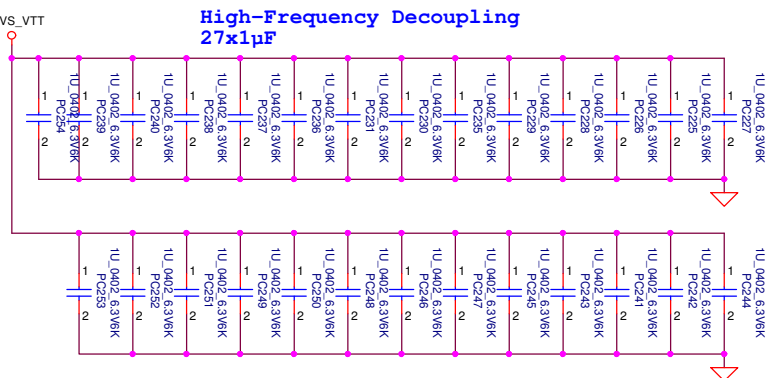
Mid-Frequency Decoupling
12x22 μ F



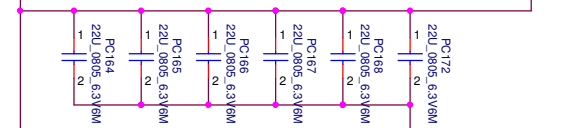
Low-Frequency
Decoupling 3x330 μ F 9m



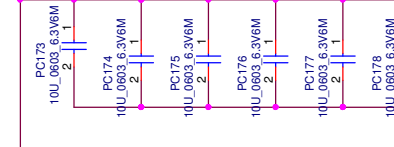
High-Frequency Decoupling
16x2.2μF



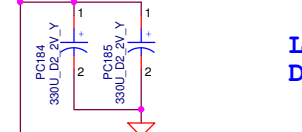
Mid-Frequency Decoupling
6x22μF



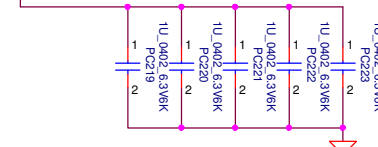
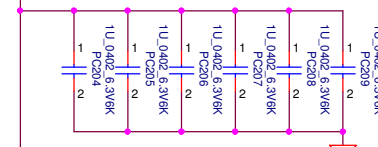
Mid-Frequency Decoupling
6x10 μ F 0603



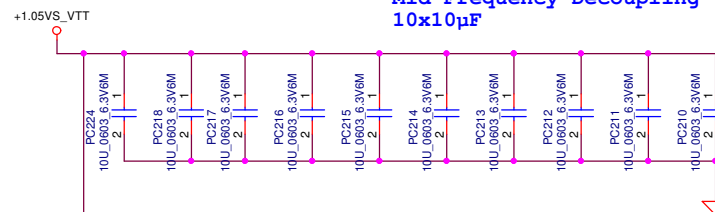
Low-Frequency
Decoupling 2x330 μ F 9m



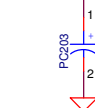
High-Frequency Decoupling
11x1 μ F



Mid-Frequency Decoupling
10x10 μ F



Low-Frequency
Decoupling 1x330 μ F 9m



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1			0.1			2010/12/29	
2			0.1	---		2010/12/29	
3						2011/02/08	
4						2011/02/08	
5						2011/02/08	
6				---		2011/02/08	
7				---		2011/02/16	
8				---		2011/05/13	PVT2
9				---		2011/05/13	PVT2
10				---		2011/05/13	PVT2
11				---		2011/05/13	PVT2
12						2011/05/13	PVT2
13							
14							
15							

